STIC Search Report
EIC 2800

STIC Database Tracking Number: 130012

TO: Monica Lewis **Location: JEF 5A30** **Art Unit : 2822** **Thursday, August 19, 2004** **Case Serial Number: 10/604907**	**From: Scott Hertzog** **Location: EIC 2800** **JEF4B68** **Phone: 272-2663** **Scott.hertzog@uspto.gov**

Search Notes

Examiner Lewis,

Attached are edited first pass search results from the patent and nonpatent databases.

Colored tags indicate abstracts especially worth your review.

If you need further searching or have questions or comments, please let me know.

Thanks,
Scott Hertzog

```
     FILE 'REGISTRY' ENTERED AT 16:17:28 ON 18 AUG 2004
SET  ABB=ON  PLU=ON
L1          246 S (SI/MF OR GE/MF OR GESI/MF OR GE.SI/MF OR GE SI/ELF) AND NC=1
L2           81 S SI/MF AND NC=1
L3         7688 S ((T1 OR T2 OR T3)/PG)(P)SI/ELS(P)0/C NOT
                  (A1 OR A2 OR A7 OR A8 OR LNTH OR ACTN OR SHEL)/PG AND 1/NC

     FILE 'HCAPLUS' ENTERED AT 16:17:38 ON 18 AUG 2004
L4        95180 S MOSFET OR IGFET OR (OXIDE# OR INSULAT? OR MOS OR IG)(2A)(FET OR
                  FIELD EFFECT) OR HFET OR HEMT OR MESFET OR FET OR FETS OR
                  FIELD(W)EFFECT OR MOSFET OR IGFET OR HFET OR HEMT OR MESFET OR FIELD
                  EFFECT TRANSISTORS+NT/CT
L5       588705 S UNDERCUT? OR UNDER(A)CUT#### OR EXTENSION# OR EXTEND? OR ETCHBACK?
                  OR ETCH?(W)BACK? OR OVERHANG? OR OVER(A)HANG? OR VOID? OR HOLLOW? OR
                  NOTCH?
L6       210603 S RECESS? OR INDENT? OR DEPRES?
L7       365275 S CHANNEL## OR TROUGH? OR TRENCH## OR GROOV##
L8         6125 S (S OR STRAIN?)(A)(SI OR SILICON OR L2) OR SSI
L9        39718 S POLYSI OR POLYSILICON? OR (MICROCRYST? OR POLYCRYST? OR (POLY OR
                  MICRO)(W)CRYSTAL? OR POLY)(W)(SILICON? OR SI OR L2)
L10       61359 S L3 OR SILICID? OR SALICID? OR WSI OR COSI OR NISI OR TASI OR TISI
L11        9788 S SOI OR (SILICON OR SI)(W)INSULATOR?
L12     3737665 S NM OR ANG OR ANGS OR ANGST? OR THICK? OR THIN? OR MICRON? OR MU OR
                  MILLIMICRO? OR MMU OR DIMEN? OR DISTANCE? OR WIDTH? OR LENGTH? AA OR
                  NANOMET? OR MUM OR ULTRATHIN? OR SUPERTHIN? OR VERYTHIN? OR
            NANOTHICK?
L13          56 S L4 AND L5 AND L6 AND L7
L14          33 S L13 AND (L8 OR L9 OR L10 OR L11 OR L12)
L15           4 S L14 AND L11
L16           1 S L15 NOT P/DT NOT PY>2003
                D .HCAPLUS IND
L17           3 S L15 AND P/DT
                D 1-3 .PATRN IND
L18           9 S L14 NOT L15 NOT P/DT NOT PY>2003
                D 1-9 .HCAPLUS IND
L19          20 S L14 AND P/DT NOT L17
                D 1-20 .PATRN IND
ANSWER SET L14 HAS BEEN SAVED AS 'A604907/A'
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     FILE 'INSPEC, COMPENDEX' ENTERED AT 09:21:40 ON 19 AUG 2004
SET  ABB=ON  PLU=ON
                ACTIVATE A604907/A
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L1              QUE SI/MF AND NC=1
L2              QUE ((T1 OR T2 OR T3)/PG)(P)SI/ELS(P)0/C NOT
                (A1 OR A2 OR A7 OR A8 OR LNTH OR ACTN OR SHEL)/PG AND 1/NC
L3              QUE MOSFET OR IGFET OR (OXIDE# OR INSULAT? OR
                MOS OR IG)(2A)(FET OR FIELD EFFECT) OR HFET OR HEMT OR MESFET
                OR FET OR FETS OR FIELD(W)EFFECT OR MOSFET OR IGFET OR HFET OR
                HEMT OR MESFET OR FIELD EFFECT TRANSISTORS+NT/CT
L4              QUE UNDERCUT? OR UNDER(A)CUT#### OR EXTENSION#
                OR EXTEND? OR ETCHBACK? OR ETCH?(W)BACK? OR OVERHANG? OR
                OVER(A)HANG? OR VOID? OR HOLLOW? OR NOTCH?
L5              QUE RECESS? OR INDENT? OR DEPRES?
L6              QUE CHANNEL## OR TROUGH? OR TRENCH## OR GROOV##
L7              QUE (S OR STRAIN?)(A)(SI OR SILICON OR L1) OR SSI
L8              QUE POLYSI OR POLYSILICON? OR (MICROCRYST? OR POLYCRYST? OR (POLY OR
                  MICRO)(W)CRYSTAL? OR POLY)(W)(SILICON? OR SI OR L1)
L9              QUE L2 OR SILICID? OR SALICID? OR WSI OR COSI OR NISI OR TASI OR TISI
L10             QUE SOI OR (SILICON OR SI)(W)INSULATOR?
L11             QUE NM OR ANG OR ANGS OR ANGST? OR THICK? OR
                THIN? OR MICRON? OR MU OR MILLIMICRO? OR MMU OR DIMEN? OR
                DISTANCE? OR WIDTH? OR LENGTH? AA OR NANOMET? OR MUM OR
                ULTRATHIN? OR SUPERTHIN? OR VERYTHIN? OR NANOTHICK?
L12             QUE L3 AND L4 AND L5 AND L6
L13             QUE L12 AND (L7 OR L8 OR L9 OR L10 OR L11)
               ---------
L14         29 S L3 AND L4 AND L5 AND L6 AND L11
L15       5391 S (S OR STRAIN?)(A)(SI OR SILICON) OR SSI
L16      35897 S POLYSI OR POLYSILICON? OR (MICROCRYST? OR POLYCRYST? OR (POLY OR
                  MICRO)(W) CRYSTAL? OR POLY)(W)(SILICON? OR SI)
L17          3 S L14 AND (L9 OR (L15 OR L16) OR L10)
L18         26 S L14 NOT L17

     FILE 'HCAPLUS' ENTERED AT 09:35:05 ON 19 AUG 2004
                ACTIVATE A604907/A
               ---------
L19 (       81)S SI/MF AND NC=1
L20 (     7688)S ((T1 OR T2 OR T3)/PG)(P)SI/ELS(P)0/C NOT
                  (A1 OR A2 OR A7 OR A8 OR LNTH OR ACTN OR SHEL)/PG AND 1/NC
L21 (    95180)S MOSFET OR IGFET OR (OXIDE# OR INSULAT? OR
                MOS OR IG)(2A)(FET OR FIELD EFFECT) OR HFET OR HEMT OR MESFET
                OR FET OR FETS OR FIELD(W)EFFECT OR MOSFET OR IGFET OR HFET OR
                HEMT OR MESFET OR FIELD EFFECT TRANSISTORS+NT/CT
L22 (   588705)S UNDERCUT? OR UNDER(A)CUT#### OR EXTENSION#
                OR EXTEND? OR ETCHBACK? OR ETCH?(W)BACK? OR OVERHANG? OR
                OVER(A)HANG? OR VOID? OR HOLLOW? OR NOTCH?
L23 (   210603)S RECESS? OR INDENT? OR DEPRES?
L24 (   365275)S CHANNEL## OR TROUGH? OR TRENCH## OR GROOV##
L25 (     6125)S (S OR STRAIN?)(A)(SI OR SILICON OR L19) OR SSI
L26 (    39718)S POLYSI OR POLYSILICON? OR (MICROCRYST? OR POLYCRYST? OR (POLY OR
                  MICRO)(W)CRYSTAL? OR POLY)(W)(SILICON? OR SI OR L19)
L27 (    61359)S L20 OR SILICID? OR SALICID? OR WSI OR COSI OR NISI OR TASI OR TISI
L28 (     9788)S SOI OR (SILICON OR SI)(W)INSULATOR?
```

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L29 (   3737665)S NM OR ANG OR ANGS OR ANGST? OR THICK? OR
                THIN? OR MICRON? OR MU OR MILLIMICRO? OR MMU OR DIMEN? OR
                DISTANCE? OR WIDTH? OR LENGTH? AA OR NANOMET? OR MUM OR
                ULTRATHIN? OR SUPERTHIN? OR VERYTHIN? OR NANOTHICK?
L30 (        56)S L21 AND L22 AND L23 AND L24
L31          33 S L30 AND (L25 OR L26 OR L27 OR L28 OR L29)
               ---------
                SET DUPORDER FILE
     FILE 'HCAPLUS, INSPEC, COMPENDEX' ENTERED AT 09:35:46 ON 19 AUG 2004
L32          46 DUP REM L31 L18 (13 DUPLICATES REMOVED)
                      ANSWERS '1-33' FROM FILE HCAPLUS
                      ANSWERS '34-44' FROM FILE INSPEC
                      ANSWERS '45-46' FROM FILE COMPENDEX
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130012

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 8/16/04 Serial # 10/604,907 Priority Application Date 2003 0826

Your Name M. Lewis Examiner # _____

AU 2822 Phone 272-1838 Room 5A30

In what format would you like your results? Paper is the default. (PAPER) DISK EMAIL

If submitting more than one search, please prioritize in order of ~~need~~.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

08-17-04

Where have you searched so far on this case?

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: _____

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. _____

What types of references would you like? Please checkmark:

Primary Refs ___ Nonpatent Literature ___ Other ___

Secondary Refs ___ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 1-28

Problem: See paragraphs 1-10

Solution: " " 11-14

☐ **L16 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2002:330749 HCAPLUS Full Text

Title

Characteristics of different structure sub-100 nm MOSFETs with high-k gate dielectrics

Author/Inventor

Liu, Xiaoyan; Lou, Shuzuo; Xia, Zhiliang; Guo, Dechao; Zhu, Huiwen; Kang, Jinfeng; Han, Ruqi

Source

Proceedings - International Conference on Solid-State and Integrated Circuit Technology, 6th, Shanghai, China, Oct. 22-25, 2001 (**2001**), Volume 1, 333-336. Editor(s): Li, Bing-Zong. Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y. CODEN: 69CNW6; ISBN: 0-7803-6520-8

Abstract

The extensive simulations are carried out to study impact of high K dielec. both on the ***channel*** and the source/drain ***extension*** region of a typical 70 ***nm*** ***MOSFET*** by two ***dimensional*** device simulator ISE. The key factors affecting the device characteristics are investigated. The different structures of high K gate dielec. ***MOSFETs*** including ***SOI*** ***MOSFET*** and ***recess*** ***channel*** ***MOSFET*** are also simulated.

Controlled or Index Terms

Dielectric constant
Dielectric films
Electric current-potential relationship
Leakage current
MOSFET (transistors)
SOI devices
Threshold potential
(characteristics of different structure sub-100 ***nm*** ***MOSFETs*** with high-k gate dielecs.)
7440-21-3, Silicon, uses 7631-86-9, Silica, uses
RL: DEV (Device component use); USES (Uses)
(characteristics of different structure sub-100 ***nm*** ***MOSFETs*** with high-k gate dielecs.)

Supplementary Terms

MOSFET dielec film const leakage current threshold voltage

☐ **L18 ANSWER 1 OF 9 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2004:345361 HCAPLUS Full Text

Title

Optimization of sub-50nm MOSFETs to mitigate drive current degradation due to silicon recess in S/D

Author/Inventor

Shiho, Yasuhito; Winstead, Brian; Foisy, Mark; Orlowski, Marius

Source

International Conference on Simulation of Semiconductor Processes and Devices, Boston, MA, United States, *Sept. 3-5, 2003 (2003)*, 187-190 Publisher: IEEE, New York, N. Y. CODEN: 69FHNS; ISBN: 0-7803-7826-1

Abstract

The ***recess*** of silicon in the source/drain and ***extension*** area severely compromises the performance of sub-50nm ***MOSFETs***. In this paper we investigate the influence of silicon ***recess*** on the transistor characteristics using process and device simulation, and systematically map the engineering space for

optimization of ***channel*** , halo, S/D implants, spacer formations, ***silicidation*** and integration schemes to mitigate the silicon surface gouging using response surface modeling.

☐ **L18 ANSWER 2 OF 9 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2002:855757 HCAPLUS Full Text

Title

p-Capped GaN-AlGaN-GaN high-electron mobility transistors (HEMTs)

Author/Inventor

Coffie, R.; Buttari, D.; Heikman, S.; Keller, S.; Chini, A.; Shen, L.; Mishra,

Source

Electron Device Letters (**2002**), 23(10), 588-590 CODEN: EDLEDZ; ISSN: 0741-3106

Abstract

A novel p-capped GaN-AlGaN-GaN high-electron-mobility transistor has been developed to minimize radio-frequency-to-d.c. dispersion before passivation. The novel device uses a p-GaN cap layer to screen the ***channel*** from surface potential fluctuations. A low-power reactive ion etching gate ***recess*** combined with angle evaporation of the gate metal has been used to prevent gate ***extension*** and maintain breakdown voltage. Devices with gate lengths of 0.7 μ m have been produced on sapphire. Current-gain cutoff frequencies ($f\tau$) of 20 GHz and maximum frequencies of oscillation (fmax) of 38 GHz have been achieved. Unpassivated device demonstrated a saturated output power of 3.0 W/mm and peak power-added efficiency of 40% at 4.2 GHz (VDS = +20 V).

Controlled or Index Terms

High-electron-mobility transistors

(fabrication and characterization of p-capped GaN-AlGaN-GaN high-electron-mobility transistors)

25617-97-4, Gallium nitride 181508-14-5, Aluminum gallium nitride (Al0.45Ga0.55N)

RL: DEV (Device component use); USES (Uses)

(fabrication and characterization of p-capped GaN-AlGaN-GaN high-electron-mobility transistors)

Supplementary Terms

aluminum gallium nitride capped high electron mobility transistor; gallium nitride capped high electron mobility transistor

☐ **L18 ANSWER 3 OF 9 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2001:83012 HCAPLUS Full Text

Title

Analysis of a novel elevated source drain MOSFET with reduced gate-induced drain-leakage current

Author/Inventor

Kim, Kyung-Whan; Choi, Chang-Soon; Choi, Woo-Young

Source

Proceedings - IEEE Hong Kong Electron Devices Meeting, 7th, Pokfulam, China, June 24, 2000 (**2000**), 36-39 Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y. CODEN: 69AWMD

Abstract

A new self-aligned ESD (Elevated Source Drain) ***MOSFET*** structure which can effectively reduce the GIDL (Gate-Induced Drain Leakage) current is proposed and analyzed. Proposed ESD structure is characterized by sidewall spacer ***width*** (WS) and ***recessed*** - ***channel*** depth (XR) which are determined by dry-etching

process. Elevation of the Source/Drain ***extension*** region is realized so that the low-activation effect caused by low-energy ion implantation can be avoided. The GIDL current in the proposed ESD structure is reduced as the region with the peak elec. field is shifted toward the drain side.

Controlled or Index Terms

Leakage current

MOSFET (transistors)

(anal. of novel elevated source drain ***MOSFET*** with reduced gate-induced drain-leakage current)

Supplementary Terms

elevated source drain ***MOSFET*** drain leakage current

☐ **L18 ANSWER 4 OF 9 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2000:856786 HCAPLUS Full Text

Title

Analysis of a novel self-aligned elevated source drain metal-oxide - semiconductor field -effect transistor with reduced gate-induced drain leakage current and high driving capability

Author/Inventor

Kim, Kyung-Whan; Choi, Chang-Soon; Choi, Woo-Young

Source

Japanese Journal of Applied Physics, Part 1: Regular Papers, Short Notes & Review Papers (**2000**), 39(11), 6208-6211 CODEN: JAPNDE; ISSN: 0021-4922

Abstract

A new self-aligned elevated source drain metal-***oxide*** -semiconductor ***field*** - ***effect*** transistor (***MOSFET***) structure which can effectively reduce the gate-induced drain leakage current without sacrificing the driving capability is proposed and analyzed. Proposed self-aligned elevated source drain structure is characterized by sidewall spacer ***width*** and ***recessed*** - ***channel*** depth which are determined by dry etching process. Elevation of the source/drain ***extension*** region is realized so that the low-activation effect caused by low-energy ion implantation can be avoided. The gate-induced drain leakage current in the proposed self-aligned elevated source drain structure is reduced as the region with the peak elec. field is shifted toward the drain side.

Controlled or Index Terms

Drain current

Leakage current

MOSFET (transistors)

(anal. of self-aligned elevated source drain ***MOSFET*** with reduced gate-induced drain leakage current and high driving capability)

Supplementary Terms

MOSFET self aligned elevated source drain

☐ **L18 ANSWER 5 OF 9 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1997:200072 HCAPLUS Full Text

Title

Impact of gate recess offset on pseudomorphic HEMT performance: a simulation study

Author/Inventor

Asenov, A.; Babiker, S.; Cameron, N.; Taylor, M. R. S.; Beaumont, S. P.

Source

ESSDERC'96, Proceedings of the European Solid State Device Research Conference,

26th, Bologna, Sept. 9-11, 1996 (1996), 1017-1020. Editor(s): Baccarani, Giorgio; Rudan, M. Publisher: Editions Frontieres, Gif-sur-Yvette, Fr. CODEN: 64CSAW

Abstract

In this paper, using carefully calibrated numerical simulations, we investigate the effect of the gate ***recess*** offset in short ***channel*** Pseudomorphic ***HEMTs*** (PsHEMTs) on the small signal equivalent circuit components and on the overall device performance. We found that although the cut-off frequency fT of the investigated PsHEMTs has a maximum at 30 ***nm*** ***recess*** offset, fmax increases monotonously with the lateral ***extension*** of the offset.

Controlled or Index Terms

High-electron-mobility transistors
(simulation of the impact of gate ***recess*** offset on pseudomorphic ***HEMT***)

Supplementary Terms

pseudomorphic ***HEMT*** performance gate ***recess*** simulation

☐ **L18 ANSWER 6 OF 9 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1994:669010 HCAPLUS Full Text

Title

Delay of field collapse in photoconductive gaps fabricated on GaAs/AlGaAs MODFET material

Author/Inventor

Sheridan, J. A.; Nechay, B. A.; Bloom, D. M.; Solomon, P. M.; Pao, Y. C.

Source

Proceedings - IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits (**1993**) 391-400 CODEN: PIDCEA; ISSN: 1079-4700

Abstract

The authors report the fabrication of a 1 μ m photoconductive gap voltage step generator with constant output voltage of 0.10 V for 100 ps and a 2 ps rise time. The photoconductor is fabricated on GaAs/AlGaAs MODFET material and uses the two-***dimensional*** electron gas in the ***FET*** ***channel*** as the conductive medium. It is fully process-compatible with MODFETs. In devices with standard ohmic contacts, the output current stayed constant for up to 50 ps, even though the elec. field in the gap is expected to collapse in <1 ps. Two-***dimensional*** device simulations show that, although the field in the gap does collapse on the expected time scale, the current is initially determined by the contacts. A new photoconductor design, in which the ohmic contacts are laterally ***recessed*** from the etched gap region, further delayed field collapse, ***extending*** constant voltage operation to 100 ps.

Controlled or Index Terms

Transistors
(***field -effect , modulation -doped***
; delay of field collapse in photoconductive gaps fabricated on GaAs/AlGaAs MODFET material)
Photoconductors
Simulation and Modeling, physicochemical
(delay of field collapse in photoconductive gaps fabricated on GaAs/AlGaAs MODFET material)
37264-06-5, Germanium gold nickel 58049-07-3, Gold, titanium
RL: DEV (Device component use); USES (Uses)
(delay of field collapse in photoconductive gaps fabricated on GaAs/AlGaAs MODFET material)
1303-00-0P, Gallium arsenide, uses 106495-76-5P, Aluminum gallium

arsenide (al0.25ga0.75as)
RL: DEV (Device component use); SPN (Synthetic preparation); PREP (Preparation); USES (Uses)
(delay of field collapse in photoconductive gaps fabricated on GaAs/AlGaAs MODFET material)

Supplementary Terms

photoconductor gallium arsenide aluminum gallium arsenide; modulation doped ***field effect*** transistor; photoconductive gap field collapse simulation

☐ **L18 ANSWER 7 OF 9 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1994:496985 HCAPLUS Full Text

Title

The applications of citric acid/hydrogen peroxide etching solutions in the processing of pseudomorphic MODFETs

Author/Inventor

Mao, B. Y.; Nielsen, J. A.; Friedman, R. A.; Lee, G. Y.

Source

Journal of the Electrochemical Society (**1994**), 141(4), 1082-5 CODEN: JESOAN; ISSN: 0013-4651

Abstract

The etching characteristics of GaAs and Al0.28Ga0.72As in citric acid/H2O2 etching solution were studied. The etch rate and the selectivity were measured over a wide concentration range from room temperature down to 0°. By changing the concentration of the solution the authors can vary the selectivity (GaAs etch rate: Al0.28Ga0.72As etch rate) from over 80:1 to reverse selectivity of 1:1.4; the GaAs etch rate can also be varied from over 4000 Å /min to <150 Å /min. However, high selectivity process consistently shows high GaAs etch rate. The authors have developed mesa and gate ***recess*** etch processes for pseudomorphic modulation doped ***field effect*** transistor (MODFET) structures based on these results. Using a 2-step mesa etch process, the authors can produce a ***recessed*** sidewall profile of the InGaAs ***channel*** layer and hence avoid the parasitic gate leakage path caused by the contact of Schottky gate to the exposed ***channel*** layer at the sidewall. A nonselective low etch rate process was chosen for gate ***recess*** etch since the selective etch shows high GaAs etch rate and causes excessive ***undercut*** in the cap layer. Using the citric acid/H2O2 etch process with low etch rate, very uniform threshold voltage (with a standard deviation of 25 mV across a 2 in wafer) can be achieved. This is the best result reported using nonselective wet etch and compares very favorably to published results using dry etch.

Controlled or Index Terms

Transistors
(***field -effect , modulation -doped***
, aluminum gallium arsenide/gallium arsenide prepared by etching with citric acid-hydrogen peroxide solution)
Etching
Kinetics of etching
(of aluminum gallium arsenide and gallium arsenide by citric acid-hydrogen peroxide solution)
77-92-9, Citric acid, reactions 7722-84-1, Hydrogen peroxide, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(etching of aluminum gallium arsenide and gallium arsenide by solution containing)
1303-00-0, Gallium arsenide (GaAs), reactions 106097-51-2, Aluminum gallium arsenide (Al0.28Ga0.72As)

RL: RCT (Reactant); RACT (Reactant or reagent)
(etching of, by citric acid-hydrogen peroxide solution)

Supplementary Terms

etching gallium arsenide citric acid; hydrogen peroxide etching aluminum gallium arsenide; MODFET etching arsenide; modulation doped ***FET*** prepn; transistor ***field effect*** gallium arsenide

☐ **L18 ANSWER 8 OF 9 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1988:519470 HCAPLUS Full Text

Title

Sub-half micrometer gate lift-off by three layer resist process via electron beam lithography for gallium arsenide monolithic microwave integrated circuits (MIMICs)

Author/Inventor

Nagarajan, Rao M.; Rask, Steven D.; King, Michael R.; Yard, Thomas K.

Source

Proceedings of SPIE-The International Society for Optical Engineering (**1988**), 923(Electron-Beam, X-Ray, Ion-Beam Technol.: Submicrometer Lithogr. 7), 194-200
CODEN: PSISDG; ISSN: 0277-786X

Abstract

A 3-layer resist process for gate lift-off on GaAs MIMIC's by electron beam and optical lithogs. are described. The electron beam lithog. process consists of poly(di-Me glutarimide) (PMGI) as the planarizing layer, a plasma enhanced chemical vapor deposition Si nitride (SiN) as an intermediate barrier layer and PMMA as the top imaging layer. The PMMA is electron exposed and developed in MeCOEt/iso-PrOH. The pattern is then transferred to the SiN layer by CF4/O2 plasma etching. The SiN layer is then used as the mask to transfer the pattern to the PMGI layer by O2 reactive ion etching until the GaAs is exposed. The various processing parameters are optimized to obtain lip or ***overhang*** suitable for lift-off with 0.20 um gate ***dimension***. After the GaAs was ***recessed*** (to reduce the parasitic source resistance), a ***thick*** 9000 Å Ti/Pt/Au gate metal was evaporated and the unwanted gate metal is lifted off using PMGI stripper. To use the 3-layer resist process in optical litnog., the PMGI planarizing layer and SiN layer are used along with optical photoresist AZ1450J as a top imaging layer. The process levels such as mesa, source/drain, contact and metal levels for GaAs MIMICs are defined by UV lithog. (Karl Suss contact aligner) using single layer photoresist. A high overlay accuracy was obtained by use of Au metal bumps as registration marks for aligning the electron beam exposed gate to optically exposed source/drain ***channel***. Thus a higher throughput and better linewidth control are obtained using electron beam/optical lithog. techniques. This approach is currently used to fabricate a 0.20 μm gate metal semiconductor ***field effect*** transistor on GaAs.

Controlled or Index Terms

Lithography
(electron-beam, in gallium arsenide monolithic microwave integrated circuit fabrication)
Electric circuits
(integrated, gallium arsenide monolithic microwave, submicron gate lift-off by three-layer resist process for lithog. fabrication of)
74-82-8, Methane, uses and miscellaneous 7782-44-7, Oxygen, uses and miscellaneous
RL: USES (Uses)
(in plasma etching electron-beam lithog. process for fabrication of gallium arsenide monolithic microwave integrated circuit)
110-89-4, Piperidine, derivs., polymers 9011-14-7, PMMA 12033-60-2,

Silicon nitride 81458-15-3, AZ1450J
RL: USES (Uses)
(in submicron gate lift-off three-layer resist process for gallium arsenide monolithic microwave integrated circuit fabrication)
1303-00-0, Gallium arsenide, uses and miscellaneous
RL: USES (Uses)
(monolithic microwave integrated circuit fabrication using, submicron gate lift-off three-layer resist process for)

Supplementary Terms
electron lithog submicron gate lift off; gallium arsenide gate lift off lithog; integrated circuit microwave monolithic lithog; resist integrated circuit microwave monolithic

☐ **L18 ANSWER 9 OF 9 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number
1985:158769 HCAPLUS Full Text

Title
Analysis of an anomalous subthreshold current in a fully recessed oxide MOSFET using a three-dimensional device simulator

Author/Inventor
Shigyo, Naoyuki; Dang, Ryo

Source
IEEE Transactions on Electron Devices (**1985**), ED-32(2), 441-5 CODEN: IETDAI; ISSN: 0018-9383

Abstract
A 3-***dimensional*** device simulator, TOPMOST, and its use in the anal. of the anomalous subthreshold current "hump" in a fully ***recessed*** oxide MOS structure are described. The mechanism underlying the hump is clarified, and the dependence on structure parameters, such as ***channel width*** , gate oxide ***thickness*** , and gate ***extension*** , are discussed. The hump can be suppressed by a side-wall implantation.

Controlled or Index Terms
Transistors
(***field -effect*** , anomalous subthreshold current in

Supplementary Terms
transistor MOS simulator subthreshold current

☐ **L17 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2002:925723 HCAPLUS Full Text

Title

Low output-capacitance and high withstand-voltage Semiconductor devices having horizontal depression MOSFETs and fabrication of devices thereof

Author/Inventor

Shirai, Yoshifumi

Patent Assignee/Corporate Source

Matsushita Electric Works, Ltd., Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2002353462	A2	20021206	2001-158341	20010528

Abstract

The title devices comprise a 1st conductivity-type semiconductor/insulator ***SOI*** substrate, a 1st conductivity-type region formed on a source-side of the 1st conductivity-type semiconductor layer, a 2nd conductivity-type region formed on a drain-side of the 1st conductivity-type semiconductor layer, and a gate electrode in a region across between the 1st and 2nd conductivity-type regions on the 1st conductivity-type semiconductor layer. A ***channel*** is provide on the gate-electrode/1st conductivity-region overlapped region. The ***overhang*** length by the gate-electrode/2nd conductivity-region overlapped region is shorter than 0.8-times of the 1st conductivity-type semiconductor layer ***thickness***. The device arrangement gives the semiconductor devices low output capacitance and high withstand voltage even on ***thick*** semiconductor layer.

Controlled or Index Terms

Semiconductor devices
(***depression MOSFETs***; low output-capacitance and high withstand-voltage Semiconductor devices having horizontal ***depression MOSFETs*** and fabrication of devices thereof)

MOSFET (transistors)
(***depression*** ; low output-capacitance and high withstand-voltage Semiconductor devices having horizontal ***depression MOSFETs*** and fabrication of devices thereof)

Doping
(low output-capacitance and high withstand-voltage Semiconductor devices having horizontal ***depression MOSFETs*** and fabrication of devices thereof)

Electric capacitance
(output; low output-capacitance and high withstand-voltage Semiconductor devices having horizontal ***depression MOSFETs*** and fabrication of devices thereof)

Electric insulators
(semiconductor/insulator ***SOI*** ; low output-capacitance and high withstand-voltage Semiconductor devices having horizontal ***depression MOSFETs*** and fabrication of devices thereof)

7440-42-8, Boron, uses 7723-14-0, Phosphorus, uses
RL: MOA (Modifier or additive use); USES (Uses)
(low output-capacitance and high withstand-voltage Semiconductor devices having horizontal ***depression MOSFETs*** and fabrication of devices thereof)

7440-21-3, Silicon, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)

(semiconductor/insulator ***SOI***; low output-capacitance and high withstand-voltage Semiconductor devices having horizontal ***depression MOSFETs*** and fabrication of devices thereof)

Supplementary Terms

low output capacitance high withstand voltage

International Patent Classification

ICM H01L029-786

☐ **L17 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2001:573522 HCAPLUS Full Text

Title

Method for preventing trench fill erosion in semiconductor devices

Author/Inventor

Mendicino, Michael A.

Patent Assignee/Corporate Source

Motorola, Inc., USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6271143	B1	20010807	1999-306029	19990506

Abstract

A ***trench*** for isolation is formed in a substrate through an opening in a nitride masking layer. After the ***trench*** is formed, the opening in the nitride masking layer is widened uniformly by an isotropic etch. This leaves the nitride masking layer uniformly ***recessed*** from the edge of the ***trench***. The ***trench*** is then filled with oxide and, with CMP, is ***etched back*** so that there is a nearly planar surface with oxide ***extending*** outside the ***trench*** wall along the surface and abutting the ***recessed*** nitride masking layer. The nitride masking layer is then removed so that there is left an oxide overlap portion which ***extends*** outside the ***trench*** wall. Subsequent oxide etches which are required for formation of transistors etch the oxide overlap portion instead of etching down into the oxide along the sidewall of the ***trench*** whereby an improved device is formed.

Controlled or Index Terms

Polishing
(chemical-mech.; method for preventing ***trench*** fill erosion in semiconductor devices)
Electric insulators
(isolation; method for preventing ***trench*** fill erosion in semiconductor devices)
Coating materials
(masking; method for preventing ***trench*** fill erosion in semiconductor devices)
Antireflective films
Etching
Etching masks
MOSFET (transistors)
SOI devices
Semiconductor device fabrication
Semiconductor memory devices
Transistors
(method for preventing ***trench*** fill erosion in semiconductor devices)
7664-38-2, Phosphoric acid, processes

RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(etchant; method for preventing ***trench*** fill erosion in semiconductor devices)
7440-21-3, Silicon, uses 7631-86-9, Silica, uses 11105-01-4, Silicon nitride oxide 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(method for preventing ***trench*** fill erosion in semiconductor devices)
10028-15-6, Ozone, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method for preventing ***trench*** fill erosion in semiconductor devices)
78-10-4, Tetraethoxysilane
RL: TEM (Technical or engineered material use); USES (Uses)
(method for preventing ***trench*** fill erosion in semiconductor devices)

Supplementary Terms

semiconductor device fabrication prevention ***trench*** fill erosion

International Patent Classification

ICM H01L021-311

☐ **L17 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1998:766487 HCAPLUS Full Text

Title

Fabricating a field-effect transistor utilizing a SOI substrate

Author/Inventor

Soutome, Yoshihiro

Patent Assignee/Corporate Source

Sharp Kabushiki Kaisha, Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
EP 880169	A1	19981125	1998-303090	19980422
JP 11040817	A2	19990212	1998-78759	19980326
JP 3382840	B2	20030304		
TW 396635	B	20000701	1998-87105916	19980417
US 6010921	**A**	**20000104**	1998-62741	19980420

Abstract

To form a ***recess*** defining a ***channel*** region in a ***SOI*** layer, a LOCOS oxide film is formed on a surface of the ***SOI*** layer and then removed. Then, side walls of CVD oxide are formed on side surfaces defining an opening of a LOCOS oxide restraining film. Then, a gate oxide film is formed on an exposed surface of the ***SOI*** layer inside the opening. CVD ***polycryst. Si*** is formed on the whole wafer surface, and then ***etched back*** to form a gate electrode of ***polycryst. Si*** inside the opening. At this time, the top surface of the gate electrode is lower than the top surface of the restraining film. Next, the restraining film and the side walls are removed and ion implantation into the ***SOI*** layer is performed using the gate electrode as a mask to form source and drain regions. Then, side walls are formed on the side surfaces of the gate electrode, and a ***silicide*** film is formed on the gate electrode and the source and drain regions.

Controlled or Index Terms

Vapor deposition process
(chemical; in fabricating a ***field -effect*** transistor utilizing a ***SOI*** substrate)
Electric ***insulators***
Field effect transistors
Semiconductor device fabrication
(fabricating a ***field -effect*** transistor utilizing a ***SOI*** substrate)
Silicides
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabricating a ***field -effect*** transistor utilizing a ***SOI*** substrate containing)
Oxidation
(formation of a LOCOS oxide film in fabricating a ***field -effect*** transistor utilizing a ***SOI*** substrate)
Oxides (inorganic), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(formation of a LOCOS oxide film in fabricating a ***field -effect*** transistor utilizing a ***SOI*** substrate)
Etching
Ion implantation
(in fabricating a ***field -effect*** transistor utilizing a ***SOI*** substrate)
7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabricating a ***field -effect*** transistor utilizing a ***SOI*** substrate)

Supplementary Terms

field effect transistor ***SOI*** substrate manuf

International Patent Classification

ICM H01L021-336
ICS H01L021-28

☐ **L19 ANSWER 1 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2003:497425 HCAPLUS Full Text

Title

MOSFET with buried contact short channel recessed gate

Author/Inventor

Wu, Shie-Lin

Patent Assignee/Corporate Source

Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
TW 411513	B	20001111	1998-87101597	19980206

Abstract

The device is fabrication by forming insulator pad; a stacked layer; removing part of the stacked layer, forming gate insulator, ion implantation to form doped region; removing the insulator and stacked, and form the semiconductor. Part of the semiconductor layer is removed, forming the spacer. Part of the gate insulator is removed, and ion implantation is used to for a region which prevents punch through. A 1st insulator is formed forming a gate electron. Partially removing the 1st insulator layer, ion implantation is used to form contact surface. A 2nd dielec. is formed followed by annealing. Finally metal interconnection completes the process. The device consists of substrate, gate insulator, gate electrode, gate oxide, semiconductor layer, source and drain region, ***extended*** source and drain region, and anti-punch-through region.

Controlled or Index Terms

Electric insulators
Gate contacts
Integrated circuits
Ion implantation
MOSFET (transistors)
Rapid thermal annealing
Semiconductor device fabrication
(fabrication of ***MOSFET*** with buried contact short ***channel recessed*** gate)
7440-21-3, ***Polysilicon*** , uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(fabrication of ***MOSFET*** with buried contact short ***channel recessed*** gate)
7440-38-2, Arsenic, uses 7440-42-8, Boron, uses 7723-14-0, Phosphorus, uses 11105-01-4, Silicon oxynitride
RL: MOA (Modifier or additive use); RCT (Reactant); RACT (Reactant or reagent); USES (Uses)
(fabrication of ***MOSFET*** with buried contact short ***channel recessed*** gate)

Supplementary Terms

buried contact short ***channel recessed*** gate ***MOSFET***

International Patent Classification

ICM H01L021-283

☐ **L19 ANSWER 2 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2003:454754 HCAPLUS Full Text

Title

Matrix-addressable array of integrated transistor/memory structures

Author/Inventor

Gudesen, Hans Gude

Patent Assignee/Corporate Source

Belg.

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2003107067	A1	20030612	2002-300802	20021121
US 6724028	B2	20040420		
WO 2003050814	A1	20030619	2002-NO426	20021118

Priority Application Information

NO 2001-6041	20011210
US 2001-PV338663	20011211

Abstract

In an array of integrated transistor/memory structures the array comprises one or more layers of semiconducting material, two or more electrode layers, and memory material contacting electrodes in the latter. At least one layer of a semiconducting material and two electrode layers form transistor structures such that the electrodes of the first electrode layer forms source/drain electrode pairs and those of a second electrode layer form the gate electrodes thereof. The source and drain electrodes of a single transistor/memory structure are separated by a narrow ***recess*** ***extending*** down to the semiconducting layer wherein the transistor ***channel*** is provided beneath the ***recess*** and with extremely small ***width*** , while the source and drain regions are provided beneath the resp. source and drain electrodes on either side of the transistor ***channel***. Memory material is provided in the ***recess*** and contacts the electrodes of the transistor. This arrangement defines the transistor ***channel*** with a length L corresponding to the ***width*** of the ***recess*** and a ***width*** W corresponding to the ***width*** of the gate electrode, L being a fraction of W, and three memory cells in the memory material formed resp. between the source electrode and the gate electrode, the drain electrode and the gate electrode and in the ***recess*** between the source and drain electrodes.

Controlled or Index Terms

Electrets
Ferroelectricity
Field effect transistors
Integrated circuits
Memory devices
Nonvolatile memory devices
Semiconductor materials
Transistors
(matrix-addressable array of integrated transistor/memory structures)
Polymers, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(semiconducting; matrix-addressable array of integrated transistor/memory structures)
28960-88-5, Vinylidene fluoride-trifluoroethylene copolymer
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(ferroelec.; matrix-addressable array of integrated transistor/memory structures)
135-48-8, Pentacene 7440-21-3, Silicon, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(matrix-addressable array of integrated transistor/memory structures)

Supplementary Terms

matrix addressable array integrated transistor memory structure

International Patent Classification

ICM H01L029-76
ICS H01L029-94

☐ **L19 ANSWER 3 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2003:355536 HCAPLUS Full Text

Title

Transistor structure and process to fabricate same

Author/Inventor

Wang, Zhongze

Patent Assignee/Corporate Source

USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2003085435	A1	20030508	2001-8854	20011102

Abstract

A transistor structure and method to fabricate same are presented. The semiconductor transistor structure comprises a transistor having an effective ***channel width*** that is greater than a lateral surface ***dimension*** spanned by an overlying transistor gate. The method of forming the transistor structure comprises the steps of forming at least one ***recessed*** region into a semiconductive material defined as an active area for the transistor; forming a transistor gate dielec. material directly and substantially conformally on the semiconductive material and into the at least one ***recessed*** region; and forming a transistor gate electrode substantially conformally overlying the transistor gate dielec. material and ***extending*** into the at least one ***recessed*** region such that the transistor gate electrode spans a ***width*** of the active area.

Controlled or Index Terms

Dielectric films
Field effect transistors
Gate contacts
Semiconductor device fabrication
(transistor structure and process to fabricate same)

Supplementary Terms

transistor semiconductor device fabrication

International Patent Classification

ICM H01L021-336
ICS H01L021-8234; H01L029-76; H01L031-119

☐ **L19 ANSWER 4 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2003:296042 HCAPLUS Full Text

Title

Method of forming MOSFET with buried contact and air-gap gate structure

Author/Inventor

Wu, Shye-Lin

Patent Assignee/Corporate Source

Texas Instruments-Acer Incorporated, Taiwan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6548362	B1	20030415	1999-325811	19990604

Abstract

The present invention relates to a semiconductor device process, and more specifically, to a method to form a ***MOSFET*** with buried contacts and air-gap gate structure. The method comprises the following steps: first, a gate is formed of a pad oxide layer and a nitride layer sequentially on a Si substrate, which has ***trench*** isolations. Then, a ***polysilicon*** layer and an oxide layer are deposited in order on all areas. Subsequently, the layer is ***etched back*** using the nitride layer a stopping layer. Thus, the nitride layer is removed to form a gate ***hollow*** region. After the pad oxide layer is removed, an oxynitride layer is re-grown to function as the gate oxide. Thereafter, Si is deposited on all areas to refill the gate ***hollow*** region. A planarization process is performed using the oxide layer as an etch-stop layer. Subsequently, the oxide layer is removed. The source, drain, and gate are ion implanted into the ***polysilicon*** layer and the Si layer. Then, the nitride spacers are removed to form dual ***recessed*** spaces. Another ion implantation is undertaken into the 1st doped region and in a 2nd doped region, which is in the bottom of the dual ***recessed*** spaces. A CVD oxide layer is then deposited on all areas to seal the dual ***recessed*** regions and form the air-gaps. Finally, an annealing process is carried out to form the shallow source/drain, ***extended*** source/drain junctions, and the buried contacts.

Controlled or Index Terms

Electric contacts
(buried; method of forming ***MOSFET*** with buried contact and air-gap gate structure)
Vapor deposition process
(chemical, low-pressure; method of forming ***MOSFET*** with buried contact and air-gap gate structure)
Polishing
(chemical-mech.; method of forming ***MOSFET*** with buried contact and air-gap gate structure)
Electric insulators
(isolation; method of forming ***MOSFET*** with buried contact and air-gap gate structure)
Annealing
Dielectric films
Doping
Etching
Ion implantation
MOSFET (transistors)
Semiconductor device fabrication
(method of forming ***MOSFET*** with buried contact and air-gap gate structure)
7727-37-9, Nitrogen, processes 7782-44-7, Oxygen, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(annealing ambient; method of forming ***MOSFET*** with buried contact and air-gap gate structure)
7631-86-9, Silica, uses 11105-01-4, Silicon nitride oxide 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(method of forming ***MOSFET*** with buried contact and air-gap gate structure)
7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(polycryst.; method of forming ***MOSFET*** with buried contact and air-gap gate structure)

78-10-4, Tetraethoxysilane
RL: RCT (Reactant); RACT (Reactant or reagent)
(vapor deposition precursor; method of forming ***MOSFET*** with buried contact and air-gap gate structure)

Supplementary Terms

semiconductor device ***MOSFET*** transistor buried contact air gap gate

International Patent Classification

ICM H01L021-336
ICS H01L021-3205; H01L021-4763

☐ **L19 ANSWER 5 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2003:152651 HCAPLUS Full Text

Title

Field-effect transistors having recessed gates and fabrication of FETs

Author/Inventor

Suemitsu, Tetsuya; Ishii, Tetsuyoshi

Patent Assignee/Corporate Source

Nippon Telegraph and Telephone Corp., Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 2003059944	A2	20030228	2001-241071	20010808

Abstract

The title ***FETs*** comprise a ***channel*** layer formed on a semiconductor substrate, a Schottky junction layer formed on the ***channel*** layer, an insulator film having a main gate opening provided in the center of the film and an unsym. gate opening, a T-shaped gate contact formed on the insulator film and ***extended*** down through the gain gate opening of the insulator film to contact the top of the Schottky junction layer, a drain contact on the unsym. gate opening-side of the insulator film on the contact layer, and a source contact at the edge of the insulator film in opposition position to the drain contact. The opening diameter size of the unsym. gate opening is less than that of the insulator film ***thickness***. The opening for the contact layer for the T-gate contact is formed by isotropic wet etching with an acid such as citric acid to give ***recess*** regions with differentiated ***widths***.

Controlled or Index Terms

Field effect transistors
(***HFETs*** ; ***field -effect*** transistors having ***recessed*** gates and fabrication of ***FETs***)
Gate contacts
(T-shaped ***recessed*** ; ***field -effect*** transistors having ***recessed*** gates and fabrication of ***FETs***)
Etching
Schottky semiconductor junctions
(***field -effect*** transistors having ***recessed*** gates and fabrication of ***FETs***)
106070-23-9, Aluminum indium arsenide ((Al,In)As)
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(buffer/Schottky; ***field -effect*** transistors having ***recessed*** gates and fabrication of ***FETs***)
9011-14-7
RL: NUU (Other use, unclassified); PRP (Properties); USES (Uses)

(electron resist layer; ***field -effect*** transistors having ***recessed*** gates and fabrication of ***FETs***)
77-92-9, Citric acid, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(etchant; ***field -effect*** transistors having ***recessed*** gates and fabrication of ***FETs***)
7440-21-3, Silicon, uses
RL: MOA (Modifier or additive use); USES (Uses)
(***field -effect*** transistors having ***recessed*** gates and fabrication of ***FETs***)
22398-80-7, Indium phosphide, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(semiconductor substrate; ***field -effect*** transistors having ***recessed*** gates and fabrication of ***FETs***)

Supplementary Terms

gate contact ***recess*** unsymmetry differential ***width*** ***FET*** fabrication

International Patent Classification

ICM H01L021-338
ICS H01L029-778; H01L029-812

☐ **L19 ANSWER 6 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2002:461263 HCAPLUS Full Text

Title

Method for making borderless contacts to active device regions and overlaying shallow trench isolation regions in integrated circuit

Author/Inventor

Huang, Jenn Ming

Patent Assignee/Corporate Source

Taiwan Semiconductor Manufacturing Company, Taiwan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6406987	B1	20020618	1998-149258	19980908

Abstract

A method for making borderless contacts to source/drain areas that overlap the shallow ***trench*** isolation (STI) is achieved. The method reduces contact shorts between the source/drain and the substrate, and eliminates erosion of the gate oxide to prevent gate/drain shorts. The method involves forming ***trenches*** in a silicon substrate, which are filled with a SiO2 and ***etched back*** to form STI surrounding and elec. isolating device areas. The STI is essentially planar with the substrate surface. A gate oxide is formed on the device areas and a ***polysilicon*** (or polycide layer) is patterned to form ***FET*** gate electrodes. A first Si3N4 layer is deposited and ***etched back*** to form sidewall spacers on the gate electrodes. The STI is ***recessed*** using a dip etch. A ***thin*** stress-release oxide is formed and a second Si3N4 layer is deposited and ***etched back*** to form visors (protective coverings) on the exposed sidewalls of the ***trench***. An interlevel dielec. is deposited and borderless contact openings that ***extend*** over the STI can now be etched to the active device areas to provide improved circuit d. When metal plugs are formed in the contact openings, the visor protects the source/drain contacts and the underlying substrate from elec. shorting.

Controlled or Index Terms

Memory devices

(DRAM (dynamic random access); making borderless contacts to active device regions and overlaying shallow ***trench*** isolation regions in integrated circuit)
Memory devices
(SRAM (static random access); making borderless contacts to active device regions and overlaying shallow ***trench*** isolation regions in integrated circuit)
Vapor deposition process
(chemical; making borderless contacts to active device regions and overlaying shallow ***trench*** isolation regions in integrated circuit)
MOS devices
(complementary; making borderless contacts to active device regions and overlaying shallow ***trench*** isolation regions in integrated circuit)
Sputtering
(etching, reactive; making borderless contacts to active device regions and overlaying shallow ***trench*** isolation regions in integrated circuit)
Electric contacts
Etching
Field effect transistors
Integrated circuits
Ion implantation
Semiconductor device fabrication
(making borderless contacts to active device regions and overlaying shallow ***trench*** isolation regions in integrated circuit)
Etching
(sputter, reactive; making borderless contacts to active device regions and overlaying shallow ***trench*** isolation regions in integrated circuit)
7440-21-3, Silicon, uses 7440-42-8, Boron, uses 7631-86-9, Silica, uses 12033-89-5, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(making borderless contacts to active device regions and overlaying shallow ***trench*** isolation regions in integrated circuit)

Supplementary Terms

integrated circuit borderless contact manuf active region shallow ***trench***

International Patent Classification

ICM H01L021-22

☐ **L19 ANSWER 7 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2002:392101 HCAPLUS Full Text

Title

Semiconductor device having field effect transistor with buried gate electrode surely overlapped with source region and process for fabrication thereof

Author/Inventor

Maruoka, Michiaki

Patent Assignee/Corporate Source

Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2002060339	A1	20020523	2001-988964	20011119
JP 2002158355	A2	20020531	2000-353072	20001120

Priority Application Information

JP 2000-353072	20001120

Abstract

A buried gate type power ***FET*** has a drain layer forming a lower part of a Si substrate, a base layer forming another part of the Si substrate on the lower part, a source region forming a surface portion of the Si substrate on the another part, a gate insulating layer covering an inner surface of a ***groove*** penetrating from the surface of the Si substrate through the source region and the base region into the drain region and a ***poly -Si*** gate electrode filling the secondary ***groove*** defined by the gate insulating layer, wherein the gate electrode is formed with a ***recess*** exposed to the upper surface thereof and covered with an insulating layer defining a secondary ***recess*** filled with a piece of ***polysilicon*** so as to reduce the effective ***width*** of the gate electrode, thereby creating the upper surface substantially coplanar with the surface of the source region in spite of an ***etch back*** carried on a ***poly -Si*** layer for forming the gate electrode.

Controlled or Index Terms

Gate contacts
(buried electrode surely overlapped with source region in ***FET***)
Electrodes
(buried gate surely overlapped with source region in ***FET***)
Semiconductor device fabrication
(of ***FET*** with buried gate electrode surely overlapped with source region)
Etching
Ion implantation
(of semiconductor device having ***FET*** with buried gate electrode surely overlapped with source region)
Electric insulators
(semiconductor device having ***FET*** with buried gate electrode surely overlapped with source region)
Field effect transistors
(with buried gate electrode surely overlapped with source region)
7440-42-8, Boron, uses 12355-90-7, Difluoroboron(1+)
RL: DEV (Device component use); MOA (Modifier or additive use); (Uses)
(-implanted semiconductor device having ***FET*** with buried gate electrode surely overlapped with source region)
7440-21-3, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(polycryst.; semiconductor device having ***FET*** with buried gate electrode surely overlapped with source region)
7631-86-9, Silica, uses
RL: DEV (Device component use); USES (Uses)
(semiconductor device having ***FET*** with buried gate electrode surely overlapped with source region)

Supplementary Terms

semiconductor device ***FET*** buried gate electrode overlapped source region

International Patent Classification

ICM H01L029-76
ICS H01L029-94; H01L021-8238; H01L021-336

☐ **L19 ANSWER 8 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

2001:781346 HCAPLUS Full Text

Title

Field effect transistor structure with self-aligned raised source/drain extensions

Author/Inventor

Mistry, Kaizad R.

Patent Assignee/Corporate Source

Mistry, Kaizad, USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 2001033000	A1	20011025	2001-771306	20010126
US 2003052333	A1	20030320	2002-209554	20020730
US 6716046	B2	20040406		

Abstract

Field effect transistor structures include a ***channel*** region formed in a ***recessed*** portion of a substrate. The ***recessed channel*** portion permits the use of relatively ***thicker*** source/drain regions thereby providing lower source/drain ***extension*** resistivity while maintaining the phys. separation needed to overcome various short ***channel*** effects. The surface of the ***recessed channel*** portion may be of a rectangular, polygonal, or curvilinear shape. In a further aspect of the present invention, transistors are manufactured by a process in which a damascene layer is patterned, the ***channel*** region is ***recessed*** by etch that is self-aligned to the patterned damascene layer, and the gate electrode is formed by depositing a material over the ***channel*** region and patterned damascene layer, polishing off the excess gate electrodes material and removing the damascene layer.

Controlled or Index Terms

Etching
Field effect transistors
Polishing
Semiconductor device fabrication
Semiconductor materials
Surface structure
(***field effect*** transistor structure with self-aligned raised source/drain ***extensions***)

Supplementary Terms

self aligned source drain ***field effect*** transistor; damascene layer source drain ***field effect*** transistor

International Patent Classification

ICM H01L021-8238
ICS H01L031-119

☐ **L19 ANSWER 9 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1999:779199 HCAPLUS Full Text

Title

Ultrathin spacers formed laterally adjacent to a gate conductor recessed below the upper surface of a substrate

Author/Inventor

Gardner, Mark I.; Fulford, H. Jim, Jr.

Patent Assignee/Corporate Source

Advanced Micro Devices, Inc., USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5998288	A	19991207	1998-62095	19980417

Abstract

An integrated circuit fabrication process is provided for forming relatively ***thin*** sidewall spacers ***extending*** laterally from the upper portions of opposed sidewall surfaces of a transistor gate conductor which resides partially within a ***trench*** of a semiconductor substrate. The invention contemplates etching a ***trench*** through a masking layer and partially through a Si-based substrate under the masking layer. A gate dielec. is then formed on Si-based surfaces which border the ***trench***. A conformal dielec. layer is deposited across the masking layer and the gate dielec., followed by the deposition of a gate conductor material across the dielec. layer. The gate conductor material and the dielec. layer are removed from above the upper surface of the masking layer. Portions of the dielec. layer interposed between the masking layer and the gate conductor are etched to a level commensurate with the substrate surface. A LDD implant self-aligned to the lateral boundaries of the masking layer and the gate conductor sidewall surfaces ***extends*** into the substrate under the ***trench***. Relatively ***thin*** oxide spacer structures are then thermally grown on the sidewall surfaces of the gate conductor. After removing the masking layer, a source/drain implant is performed. In another embodiment, the gate conductor is formed between the opposed lateral boundaries of the masking layer on the gate dielec. A source/drain implant is performed after removing the masking. Relatively ***thin*** dielec. spacers are formed on the upper portions of the sidewall surfaces of the gate conductor by depositing and anisotropically etching a dielec.

Controlled or Index Terms

MOSFET (transistors)
(fabrication of integrated circuits containing)
Electric insulators
(formation of gate dielec. in integrated circuit fabrication)
Ion implantation
Rapid thermal annealing
(in integrated circuit fabrication)
Semiconductor device fabrication
(***ultrathin*** spacers formed laterally adjacent to a gate conductor ***recessed*** below upper surface of a substrate)
7440-21-3, Silicon, processes 7631-86-9, Silica, processes 12033-89-5, Silicon nitride (Si3N4), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of integrated circuits containing)

Supplementary Terms

ultrathin spacer formation integrated circuit fabrication; LDD implant integrated circuit fabrication

International Patent Classification

ICM H01L021-3205

☐ **L19 ANSWER 10 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1999:761141 HCAPLUS Full Text

Title

MOSFETs with recessed self-aligned silicide gradual source and drain (S/D) junction

Author/Inventor

Wu, Shye-Lin

Patent Assignee/Corporate Source

Texas Instruments-Acer Incorporated, Taiwan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5994747	A	19991130	1998-23454	19980213

Abstract

The present invention includes a gate oxide. A gate is formed on the gate oxide. ***Undercut*** portions, formed under the gate. The substrate has ***recessed*** portions are adjacent to the gate. A silicon oxynitride layer is formed on the side walls of the gate and refilled into the ***undercut*** portions to be used as a portion of the gate oxide. Side wall spacers are formed on the side walls of the gate. A polycide layer is formed at the top of the gate to reduce the elec. resistance. Source and drain regions are formed in the ***recessed*** portions of the substrate. Lightly doped drain (LDD) structures are formed in the substrate adjacent to the gate and under the gate oxide. ***Extended*** source and drain are formed between the source and drain and the LDD structure to suppress the short ***channel*** effect. Self-aligned ***silicide*** (***SALICIDE***) layers are formed at top of the source and drain.

Controlled or Index Terms

12017-12-8, Cobalt ***silicide*** (CoSi2) ***12039-88-2***, Tungsten ***silicide***
RL: DEV (Device component use); USES (Uses)
(***MOSFETs*** with ***recessed*** self-aligned ***silicide*** gradual source and drain junction)
Etching
MOSFET (transistors)
Rapid thermal annealing
Semiconductor junctions
(***MOSFETs*** with ***recessed*** self-aligned ***silicide*** gradual source and drain junction)
Silicides
RL: DEV (Device component use); USES (Uses)
(***MOSFETs*** with ***recessed*** self-aligned ***silicide*** gradual source and drain junction)
Vapor deposition process
(chemical; ***MOSFETs*** with ***recessed*** self-aligned ***silicide*** gradual source and drain junction)
7440-21-3, Silicon, uses 7631-86-9, Silica, uses 11104-62-4, Cobalt ***silicide*** 11105-01-4, Silicon nitride oxide 11129-80-9, Platinum ***silicide*** ***12017-12-8*** , Cobalt ***silicide*** (CoSi2) ***12039-88-2*** , Tungsten ***silicide*** 12627-41-7, Tungsten ***silicide*** 12738-91-9, Titanium ***silicide*** 39467-10-2, Nickel ***silicide***
RL: DEV (Device component use); USES (Uses)
(***MOSFETs*** with ***recessed*** self-aligned ***silicide*** gradual source and drain junction)

Supplementary Terms

MOSFET selfaligned ***silicide*** source drain junction

International Patent Classification

ICM H01L029-76
ICS H01L031-062

☐ **L19 ANSWER 11 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1999:505912 HCAPLUS Full Text

Title

Process of manufacturing a semiconductor device including a buried channel

field effect transistor

Author/Inventor

Frijlink, Peter; Oszustowicz, Jean-luc

Patent Assignee/Corporate Source

Koninklijke Philips Electronics N.V., Neth.; Philips Ab

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
WO 9940618	A1	19990812	1999-IB94	19990121
EP 974160	A1	20000126	1999-900239	19990121
JP 2002502557	T2	20020122	1999-540168	19990121
US 6248666	B1	20010619	1999-241017	19990201

Abstract

A process of manufacturing a semiconductor device with a double- ***recessed*** gate ***field effect*** transistor, comprising the formation, on a substrate (1), of an active layer (3) of a semiconductor material and a first dielectric layer (D1), and further comprising the steps of: forming a second dielectric layer (R), forming an aperture (A0) in the second dielectric layer (R), then a first opening (A1) in the first dielectric layer (D1) having a same first ***width*** , while forming a second opening (A2) in the second dielectric layer having a second ***width*** larger than the first ***width*** , and then etching a preliminary ***recess*** (A4) in the subjacent semiconductor layer through said first opening (A1) having said first ***width*** , enlarging said first opening (A1) in the first dielectric layer (D1) to form a third opening (A3) having a third ***width*** larger than the second ***width*** , and then etching the semiconductor layer through said preliminary ***recess*** (A4) to form a deeper central ***recess*** (A6) having substantially said first ***width*** while etching a shallower peripheral ***recess*** (A5) substantially having said third ***width*** through said third opening (A3), and depositing through said second opening (A2) a gate metal material (8) having substantially said second ***width*** and ***extending*** over said central deeper ***recess*** (A6) and partially over said peripheral shallower ***recess*** (A5).

International Patent Classification

ICM H01L021-336

ICS H01L029-78

☐ **L19 ANSWER 12 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1999:224228 HCAPLUS Full Text

Title

Forming a recessed structure for shallow trench isolation and salicide process

Author/Inventor

Wu, Sheng-Jyh; Liu, Jing-Meng; Tsai, Chao-Chieh

Patent Assignee/Corporate Source

Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5891771	A	19990406	1997-995339	19971222
US 5982017	A	19991109	1999-253293	19990219

Abstract

A shallow ***trench*** isolated ***FET*** LDD structure that has a low probability of short circuiting at the Si to ***trench*** interface or between the source or drain and the gate (because of a Ti ***silicide*** bridge) is described. It is based on an isolation ***trench*** having a top portion with vertical sides and a lower portion with sloping sides. With the filled ***trench*** in place, along with a ***polysilicon***

gate and gate oxide, a ***thinner*** , lightly doped, n-type layer is formed using ion implantation. Spacers are then formed on the gate but, prior to a 2nd ion implantation, a few hundred ***A*** of Si is selectively removed from the surface. This causes the ***trench*** filler material to ***extend*** above the wafer surface and the spacers to ***extend*** above the gate. A deeper, more strongly n-type, layer is then formed in the usual way, followed by the standard ***salicide*** process for making contact to source, gate, and drain.

Controlled or Index Terms

Field effect transistors
(forming a ***recessed*** structure for shallow ***trench*** isolation and ***salicide*** process in manufacture of)
Ion implantation
(in forming a ***recessed*** structure for shallow ***trench*** isolation and ***salicide*** process)
Silicides
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(self-aligned; forming a ***recessed*** structure for shallow ***trench*** isolation and ***salicide*** process)
7440-21-3, Silicon, processes 12738-91-9, Titanium ***silicide***
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(forming a ***recessed*** structure for shallow ***trench*** isolation and ***salicide*** process in manufacture of ***FETs*** containing)

Supplementary Terms

recessed structure shallow ***trench*** isolation ***salicide*** process

International Patent Classification

ICM H01L021-76

☐ **L19 ANSWER 13 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1997:732203 HCAPLUS Full Text

Title

High-electron-mobility transistor and its manufacture

Author/Inventor

Kamiyama, Tomoyuki

Patent Assignee/Corporate Source

Honda Giken Kogyo Kabushiki Kaisha, Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
EP 805498	A1	19971105	1997-106992	19970428
JP 09298295	A2	19971118	1996-135902	19960502

Abstract

A high-electron-mobility transistor includes a ***channel*** layer for developing a 2-***dimensional*** electron gas layer, upper and lower wide-band-gap layers disposed over and under the ***channel*** layer, and a contact layer on the upper wide-band-gap layer for contact with source and drain electrodes. The ***channel*** layer, the upper and lower wide-band-gap layers, and the contact layer are etched into a mesa structure including a side slope. The contact layer has a ***recess*** which divides the contact layer. A gate electrode is disposed in the ***recess*** and has an ***extension*** spaced in ***overhanging*** relation from the side slope by an air gap. A film of SiO2 is disposed on the side slope. The high-electron-mobility transistor also includes a superlattice buffer layer on which the lower wide-

band-gap layer is disposed, and a gate pad on the superlattice buffer layer and spaced from the mesa structure, the ***extension*** being connected to the gate pad.

Controlled or Index Terms

Etching
(in manufacture of high-electron-mobility transistors)
High-electron-mobility transistors
(manufacture of)
1303-00-0, Gallium arsenide (GaAs), processes 7440-21-3, Silicon, processes 7631-86-9, Silica, processes 106699-04-1, Aluminum gallium arsenide (Al0.2-0.3Ga0.7-0.8As)
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(manufacture of high-electron-mobility transistors containing)

Supplementary Terms

high electron mobility transistor manuf

International Patent Classification

ICM H01L029-778
ICS H01L029-423

☐ **L19 ANSWER 14 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1997:475120 HCAPLUS Full Text

Title

High-density power device fabrication using undercut oxide sidewalls

Author/Inventor

Tsang, Dah Wen; Sdrulla, Dumitru; Pike, Douglas A., Jr.; Meyer, Theodore O.; Mosier, John W. II

Patent Assignee/Corporate Source

Advanced Power Technology, Inc., USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5648283	A	19970715	1994-190325	19940131
US 5283201	A	19940201	1992-927169	19920807
WO 9403922	A1	19940217	1993-US4714	19930517
EP 654173	A1	19950524	1993-913971	19930517
US 5801417	A	19980901	1993-106406	19930813
US 2002074585	A1	20020620	2002-80871	20020222

Abstract

A ***recessed*** -gate power ***MOSFET*** on a substrate has a p-type body layer, an n-type drain layer, and an optional p+ layer for an IGBT. A layer on the surface patterns areas as stripes or a matrix, and protected areas. ***Undercut*** oxide sidewalls with protruding rims contact the sides of a ***polysilicon*** layer. A ***trench*** has Si sidewalls aligned to the oxide sidewall and ***extending*** depthwise through the p-type body layer. Gate oxide is formed on the ***trench*** walls and gate ***polysilicon*** refills the ***trench*** to a level near the surface demarcated by the ***undercut*** sidewall rims. Oxide between the spacers covers the ***polysilicon***. Removing the surface layer exposes the surface between the sidewalls. A source layer is doped on the body layer and then etched to form a ***trench*** having sidewalls aligned to the inner side faces of the sidewalls. The ***trench*** defines vertically oriented source and body layers stacked along the oxide layer to form vertical ***channels*** on opposite sides of the ***trench***. The source and body layers have the lateral ***thickness*** of the ***undercut*** sidewalls and the spacer rims. A conductor contacts the n-type source and p-type body layers and the enhanced p+ region in the ***trench***.

Controlled or Index Terms

Power semiconductor devices
(fabrication of high-d. power devices using ***undercut*** oxide sidewalls)
MOSFET (transistors)
(fabrication of high-d. power semiconductor devices using ***undercut*** oxide sidewalls)
Oxides (inorganic), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of high-d. power semiconductor devices using ***undercut*** oxide sidewalls)
Bipolar transistors
(insulated-gate; fabrication of high-d. power semiconductor devices using ***undercut*** oxide sidewalls)
7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; fabrication of high-d. power semiconductor devices containing)

Supplementary Terms

power semiconductor device manuf; ***undercut*** oxide sidewall power semiconductor device

International Patent Classification

ICM H01L021-265
ICS H01L049-00

☐ **L19 ANSWER 15 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1996:169224 HCAPLUS Full Text

Title

Fabrication of MOSFETs with silicided lightly doped drain structures

Author/Inventor

Hsu, Chen Chung

Patent Assignee/Corporate Source

United Microelectronics Corporation, Taiwan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5491099	A	19960213	1994-297497	19940829
US 5828103	A	19981027	1995-739346	19951226

Abstract

A process for fabricating ***MOSFETs*** with ***recessed*** lightly doped drains (LDD) is described. This process initially involves conventional techniques of forming a ***silicided polysilicon*** (polycide) gate structure, isolated from the ***silicided*** source and drain regions by a spacer sidewall insulator. The novel aspect of this process consists of removing the spacer insulator and etching a ***trench*** in the region between the metal ***silicided*** source/drain and the polycide gate structure. An angled ion implant is then performed to form lightly doped drain regions in the ***trench*** region, also ***extending*** under the polycide gate. This results in shortening of the ***channel*** , thus enhancing device performance.

Controlled or Index Terms

12039-83-7 , Titanium ***silicide*** (TiSi2)
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of ***MOSFETs*** with ***silicided*** lightly

doped drain structures containing)
Silicides
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of ***MOSFETs*** with ***silicided*** lightly doped drain structures)
Electric insulators and Dielectrics
(fabrication of ***MOSFETs*** with ***silicided*** lightly doped drain structures containing)
Ion beams
(implantation of; in fabrication of ***MOSFETs*** with ***silicided*** lightly doped drain structures)
Etching
(in fabrication of ***MOSFETs*** with ***silicided*** lightly doped drain structures)
Transistors
(***field -effect , MOS*** ; fabrication of ***MOSFETs*** with ***silicided*** lightly doped drain structures)
7631-86-9, Silica, processes 12033-89-5, Silicon nitride (Si3N4), processes ***12039-83-7*** , Titanium ***silicide*** (TiSi2)
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of ***MOSFETs*** with ***silicided*** lightly doped drain structures containing)
7440-21-3, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; fabrication of ***MOSFETs*** with ***silicided*** lightly doped drain structures containing)

Supplementary Terms

silicided lightly doped drain ***MOSFET*** manuf

International Patent Classification

ICM H01L021-8234

☐ **L19 ANSWER 16 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1995:330901 HCAPLUS Full Text

Title

Manufacturing a recessed insulated-gate field-effect semiconductor device

Author/Inventor

Hutchings, Keith Michael; Whight, Kenneth Ronald

Patent Assignee/Corporate Source

Philips Electronics UK Ltd., UK; N. V. Philips' Gloeilampenfabrieken

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
EP 620588	A2	19941019	1994-200834	19940329
EP 918353	A1	19990526	1999-200133	19940329
JP 06350090	A2	19941222	1994-63339	19940331
US 5378655	A	19950103	1994-221293	19940331

Abstract

A mask defining ≥1 window is provided on 1 major surface of a semiconductor body. The semiconductor body is etched to define a ***groove*** into a 1st region of 1 conductivity type through a 2nd region of the opposite conductivity type. A

relatively ***thin*** layer of gate insulator is provided on the surface of the ***groove***. A gate conductive region of an oxidizable conductive material is provided within the ***groove*** to define, with the gate insulator layer, an insulated-gate structure bounded by a conduction ***channel*** -defining area of the 2nd region. A step in the surface structure is then defined by causing the insulated-gate structure to ***extend*** beyond the surrounding surface by oxidizing the exposed gate conductive material to define an insulating capping region on the gate conductive region. A layer is formed over the surface structure and etched anisotropically to leave portions of the layer on the side wall of the step defined by the insulated-gate structure and to define beneath the portions 3rd regions of the 1 conductivity type with the 2nd region. An elec. conductive layer is deposited to contact both the 2nd and 3rd regions.

Controlled or Index Terms

Etching
Oxidation
(in manufacture of a ***recessed insulated*** -gate ***field -effect*** semiconductor device)
Semiconductor devices
(manufacture of a ***recessed insulated***-gate ***field-effect*** semiconductor device)
Transistors
(***field-effect, insulated-gate;*** manufacture of ***recessed***)

Supplementary Terms

recessed insulated gate ***field effect*** device; semiconductor device ***field effect*** manuf

International Patent Classification

ICM H01L021-336
ICS H01L029-784

☐ **L19 ANSWER 17 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1993:31471 HCAPLUS Full Text

Title

Fabrication of recess -type metal-Schottky field - effect transistors

Author/Inventor

Mitsuma, Yasuo

Patent Assignee/Corporate Source

NEC Corp., Japan

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 04171829	A2	19920619	1990-299327	19901105

Abstract

The title fabrication involves (1) forming a ***channel*** layer on a surface of a semiconductor substrate, (2) depositing a 1st insulator film on its entire surface, (3) etching to give an opening to the insulator film for preparation of a gate contact, (4) depositing a 2nd insulator film on its entire surface, (5) anisotropic ***etching back*** to form sidewalls to the opening of the 1st insulator film, (6) isotropic etching the exposed ***channel*** layer to form a ***recess*** , and (7) depositing a metal layer on its entire surface followed by selectively etching to form a Schottky gate contact from the metal layer. The ***recess*** etching gives its gate length an increased precision by elimination of unwanted ***void*** space to the gate contact in its lower portion under the 1st insulator film.

Controlled or Index Terms

Electric contacts

(gate, elimination of ***void*** in, in metal Schottky ***FET***)
Transistors
(***field-effect*** ,***recess***-type, metal
Schottky, fabrication of)
12627-41-7, Tungsten ***silicide***
RL: USES (Uses)
(gate contact, fabrication of, in metal Schottky ***FET***)

Supplementary Terms

metal Schottky ***recess*** gate contact ***FET***

International Patent Classification

ICM H01L021-338
ICS H01L021-302; H01L029-50; H01L029-812

☐ **L19 ANSWER 18 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1982:448260 HCAPLUS Full Text

Title

Low leakage shallow junction IGFET devices

Author/Inventor

Geipel, Henry J., Jr.; Shasteen, Richard B.

Patent Assignee/Corporate Source

International Business Machines Corp. , USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 4329773	A	19820518	1980-214940	19801210
JP 57097678	A2	19820617	1981-119460	19810731
EP 53683	A1	19820616	1981-108553	19811020

Abstract

A semiconductor process is disclosed for forming high-d. integrated-circuit ***insulated*** -gate ***FET*** (***IGFET***) devices having junction depths of <1 μ in which an ion implantation/diffusion process is used to provide field-oxide parasitic devices having high threshold voltages. The method is implemented in an n-***channel*** ***IGFET*** semiconductor manufacturing process by providing semi-***recessed*** field-oxide isolation regions on a semiconductor substrate, forming dielec. insulated gate electrodes in the active device region, ion implanting As ions into regions of the substrate not protected by field-oxide or gate electrodes such that the maximum concentration of As in the substrate lies substantially at the surface of the substrate, exposing the substrate to a drive-in wet oxidation process to oxidize the ion-implanted regions to a ***thickness*** greater than that of the projected range of the implanted ions, and then annealing in a nonoxidizing atmospheric at 900-1100°. The total time for the oxidation and annealing step is in excess of the time required to grow thermal oxide over the implanted regions and is determined by the ion-implant energy and dose, the oxidizing/anneal temperature, and the field-oxide ***thickness***. The ***extended*** time at temperature is necessary to reduce the effects of implanted As ions on the threshold voltage of parasitic devices formed under the field oxide and to provide for sufficient thermal diffusion of implanted As beyond O causing defects in the semiconductor substrate.

Controlled or Index Terms

Electric circuits
(silicon ***insulated*** -gate ***FET*** , fabrication of
low-leakage shallow-junction)
7440-38-2D, ions, uses and miscellaneous
RL: USES (Uses)

(implantation of, in fabrication of silicon ***insulated*** -gate ***FET*** integrated circuits)
7440-21-3, uses and miscellaneous
RL: USES (Uses)
(***insulated*** -gate ***FET*** integrated circuits, fabrication of low-leakage shallow-junction)

Supplementary Terms

silicon ***insulated*** gate ***FET*** ; integrated circuit silicon; arsenic implantation integrated circuit

International Patent Classification

H01L021-22; H01L021-26

☐ **L19 ANSWER 19 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1982:432252 HCAPLUS Full Text

Title

Field effect transistor

Author/Inventor

Godefridus, Henricus; Maas, Rafael

Patent Assignee/Corporate Source

N. V. Philips' Gloeilampenfabrieken, Neth.

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
GB 2085656	A	19820428	1981-30726	19811012
NL 8005673	A	19820503	1980-5673	19801015
CA 1171550	A1	19840724	1981-387558	19811008
DE 3140268	A1	19820616	1981-3140268	19811010
JP 57095670	A2	19820614	1981-163550	19811015
US 4937202	A	19900626	1988-272660	19881117

Abstract

Each of the source and drain regions of an ***insulated*** -gate ***FET*** is realized partly as a region in the semiconductor substrate and partly as a monocryst. part of a deposited epitaxial layer. Polycryst. parts of the epitaxial layer forming source and drain connections are separated from the substrate by an insulating layer. The ***channel*** of the transistor underlies a ***recess*** in the substrate. Thus the ***channel*** length is independent of variations in the ***thickness*** of the epitaxial layer and stray capacitances from source and drain to substrate are minimized. Moreover, for improved packing d., a conductor pattern separated from the epitaxial layer by an insulating layer may ***extend*** beyond the connections. Also, the epitaxial layer itself may comprise extra wiring tracks allowing greater freedom of circuit design. In particular, the semiconductor comprises Si and the insulating layer separating the gate electrode from the substrate comprises Si oxide. The amorphous or polycryst. layer (2-100 ***nm thick***) is deposited prior to the epitaxy at a temperature lower than that used in the subsequent epitaxy, i.e. <800°. The part of the amorphous or polycryst. layer within the aperture on the exposed semiconductor surface changes into single-crystal state by thermal treatment. At the areas of the apertures in the masking layer, impurities characteristic of the 2nd conductivity type are diffused into the substrate to a depth which is larger than the maximum ***thickness*** of the epitaxial layer.

Controlled or Index Terms

Transistors
(***field-effect***, from single crystal and ***polycryst. silicon***)

Supplementary Terms

transistor ***field effect*** silicon

International Patent Classification

H01L029-78; H01L021-18; H01L029-06

☐ **L19 ANSWER 20 OF 20 HCAPLUS COPYRIGHT 2004 ACS on STN**

Accession Number

1980:14488 HCAPLUS Full Text

Title

Narrow channel MOS devices and method of manufacturing

Author/Inventor

Sato, Shuichi; Yamaguchi, Tadanori; Ritchie, Arthur Douglas

Patent Assignee/Corporate Source

Tektronix, Inc., USA

Patent Information

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
GB 2011170	B2	19820630		
CA 1119733	A1	19820309	1978-316831	19781124
NL 7811920	A	19790625	1978-11920	19781206
FR 2412942	A1	19790720	1978-36394	19781219
US 4261761	A	19810414	1979-71965	19790904

Abstract

A method of manufacturing high performance ***MOSFETs*** adapted for large-scale integration on semiconductor substrates is described. A 400-. ***ANG.*** -***thick*** oxide layer and a 0.13-***μ-thick*** Si3N4 layer which is impermeable to O are formed on the upper surface of a p-doped monocryst. Si wafer. The Si3N4 layer is selectively etched to form a mask and the unmasked areas are locally oxidized to form a ***thick*** oxide layer ***recessed*** into the upper surface of the Si wafer. A smoothly tapered oxide beak ***extends*** between the margin of the mask and the underlying Si surface. The beak is used to vary the depth of the impurity layers subsequently formed by ion implantation.

Controlled or Index Terms

Transistors

(***field-effect***, ***MOS***, narrow-***channel***, high-performance, manufacture of)

Supplementary Terms

MOSFET high performance manuf; ***FET MOS*** high performance manuf

International Patent Classification

H01L021-265; H01L029-78

☐ **L17 ANSWER 1 OF 3 INSPEC (C) 2004 IEE on STN**

Accession Number

2004:7845882 INSPEC DN B2004-03-2560B-007 Full Text

Title

Optimization of sub-50 nm MOSFETs to mitigate drive current degradation due to silicon recess in S/D.

Author/Inventor

Shiho, Y.; Winstead, B.; Foisy, M.; Orlowski, M. (Motorola DigitaI DNA Labs., Austin, TX, USA)

Source

2003 IEEE International Conference on Simulation of Semiconductor Processes and Devices (Cat. No.03TH8679) Piscataway, NJ, USA: IEEE, 2003. p.187-90 of x+329 pp. 3 refs. Conference: Boston, MA, USA, 3-5 ***Sept 2003*** ISBN: 0-7803-7826-1

Abstract

The ***recess*** of silicon in the source/drain and ***extension*** area severely compromises the performance of sub-50 ***nm MOSFETs.*** In this paper we investigate the influence of silicon ***recess*** on the transistor characteristics using process and device simulation, and systematically map the engineering space for optimization of ***channel*** , halo, S/D implants, spacer formations, ***silicidation*** and integration schemes to mitigate the silicon surface gouging using response surface modeling.

Controlled or Index Terms

ELEMENTAL SEMICONDUCTORS; ***MOSFET*** ; OPTIMISATION; SEMICONDUCTOR DEVICE MODELS; SILICON

Supplementary Terms

optimization; ***sub-50 nm MOSFETs*** ; mitigate drive current degradation; ***Si recess in S/D*** ; source/drain area; ***extension area*** ; transistor characteristics; process and device simulation; engineering space; ***channel*** ; halo; spacer formations; ***silicidation*** ; integration schemes; response surface modeling; ***50 nm*** ; Si CHI Si int, Si el PHP size 5.0E-08 m ET S; Si

☐ **L17 ANSWER 2 OF 3 INSPEC (C) 2004 IEE on STN**

Accession Number

2002:7260564 INSPEC DN B2002-06-2560R-059 Full Text

Title

Characteristics of different structure sub-100nm MOSFETs with high-k gate dielectrics.

Author/Inventor

Xiaoyan Liu; Shuzuo Lou; Zhiliang Xia; Dechao Guo; Huiwen Zhu; Jinfeng Kang; Ruqi Han (Inst. for Microelectron., Peking Univ., Beijing, China)

Source

2001 6th International Conference on Solid-State and Integrated Circuit Technology. Proceedings (Cat. No.01EX443) Editor(s): Li, B-Z; Ru, G-P; Qu, X-P; Yu, P.; Iwai, H. Piscataway, NJ, USA: IEEE, **2001**. p.333-6 vol.1 of 2 vol.xvi+1473 pp. 5 refs. ISBN: 0-7803-6520-8

Abstract

The extensive simulations are carried out to study impact of high K dielectric both on the ***channel*** and the source/drain ***extension*** region of a typical 70nm ***MOSFET*** by the two ***dimensional*** device simulator ISE. The key factors affecting the device characteristics are investigated. The different structures of high K gate dielectric ***MOSFETs*** including ***SOI MOSFET*** and ***recess channel MOSFET*** are also simulated.

Controlled or Index Terms

MOSFET ; PERMITTIVITY; SEMICONDUCTOR DEVICE MODELS;

SILICON-ON-INSULATOR

Supplementary Terms

sub-100nm MOSFETs ; high-k gate dielectrics; ***source/drain extension region*** ; ***two dimensional device simulator ISE*** ; device characteristics; ***SOI MOSFET*** ; ***recess channel MOSFET*** ; ***100 nm*** PHP size 1.0E-07 m ET K

☐ **L17 ANSWER 3 OF 3 INSPEC (C) 2004 IEE on STN**

Accession Number

1985:2518913 INSPEC DN B85050748 Full Text

Title

A new trench isolation technology as a replacement of LOCOS.

Author/Inventor

Mikoshiba, H.; Homma, T.; Hamano, K. (NEC Corp., Kanagawa, Japan)

Source

International Electron Devices Meeting. Technical Digest (Cat. No. 84CH2099-0) New York, NY, USA: IEEE, **1984.** p.578-81 of 875 pp. 8 refs. Conference: San Francisco, CA, USA, 9-12 Dec 1984 Sponsor(s): IEEE

Abstract

The technology, which is suitable for submicron VLSI, features bird's beak-free planer surface low defect generation, and is adaptable to any isolation ***width*** from submicron to very large ***dimensions*** . The key process steps consist of filling the ***trench*** with ***polysilicon*** to half of the ***trench*** depth by utilizing photoresist ***etch back*** , and subsequent full oxidation of the ***recessed polysilicon*** to fill the ***trench*** by the oxide. Device characteristics examined experimentally are equivalent to those of LOCOS isolated devices. The feasibility of this technology has been verified successfully by fabricating a 64K bit DRAM.

Controlled or Index Terms

FIELD EFFECT INTEGRATED CIRCUITS; INTEGRATED CIRCUIT TECHNOLOGY; INTEGRATED MEMORY CIRCUITS; RANDOM-ACCESS STORAGE; VLSI

Supplementary Terms

trench isolation technology ; submicron VLSI; bird's beak-free planer surface; low defect generation; ***adaptable to any isolation width*** ; key process steps; ***photoresist etch back*** ; feasibility; 64K bit DRAM ET K

☐ **L32 ANSWER 34 OF 46 INSPEC (C) 2004 IEE on STN DUPLICATE 1**

Accession Number

2004:7853458 INSPEC DN B2004-03-1265D-025 Full Text

Title

The breakthrough in data retention time of DRAM using Recess - Channel -Array Transistor(RCAT) for 88 nm feature size and beyond.

Author/Inventor

Kim, J.Y.; Lee, C.S.; Kim, S.E.; Chung, I.B.; Choi, Y.M.; Park, B.J.; Lee, J.W.; Kim, D.I.; Hwang, Y.S.; Hwang, D.S.; Hwang, H.K.; Park, J.M.; Kim, D.H.; Kang, N.J.; Cho, M.H.; Jeong, M.Y.; Kim, H.J.; Han, J.N.; Kim, S.Y.; Nam, B.Y.; Park, H.S.; Chung, S.H.; Lee, J.H.; Park, J.S.; Kim, H.S.; Park, Y.J.; Kim, K.

Source

2003 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.03CH37407) Tokyo, Japan: Japan Soc. Applied Phys, 2003. p.11-12 of xvii+184 pp. 2 refs. Conference: Kyoto, Japan, **10-12 June 2003** ISBN: 4-89114-033-X

Abstract

For the first time, 512 Mb DRAMs using a ***Recess -Channel*** -Array-Transistor(RCAT) are successfully developed with 88 ***nm*** feature size, which is the smallest feature size ever reported in DRAM technology with non-planar array

transistor. The RCAT with gate length of 75 ***nm*** and ***recessed channel*** depth of 150 ***nm*** exhibits drastically improved electrical characteristics such as DIBL, BVDS, junction leakage and cell contact resistance, comparing to a conventional planar array transistor of the same gate length. The most powerful effect using the RCAT in DRAMs is a great improvement of data retention time. In addition, this technology will easily ***extend*** to sub-70 ***nm*** node by simply increasing ***recessed channel*** depth and keeping the same doping concentration of the substrate.

Controlled or Index Terms

CONTACT RESISTANCE; DRAM CHIPS; ELECTRICAL FAULTS; ***INSULATED GATE FIELD EFFECT TRANSISTORS***

Supplementary Terms

data retention time; ***recess channel array transistor*** ; DRAM technology; nonplanar array transistor; electrical properties; junction leakage; cell contact resistance; gate length; ***recessed channel depth*** ; doping concentration; ***88 nm*** ; ***75 nm*** ; ***150 nm*** ; ***70 nm*** PHP size 8.8E-08 m; size 7.5E-08 m; size 1.5E-07 m; size 7.0E-08 m ET B*V; BVDS; B cp; cp; V cp; D cp; S cp

☐ **L32 ANSWER 35 OF 46 INSPEC (C) 2004 IEE on STN DUPLICATE 8**

Accession Number

1990:3614695 INSPEC DN B90028726 Full Text

Title

Performance evaluation of GaAs based MODFETs.

Author/Inventor

Kohn, E.; Lepore, A.; Lee, H.; Levy, M. (Siemens Corp. Res., Princeton, NJ, USA)

Source

Proceedings. IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits (Cat. No.89CH2790-4) New York, NY, USA: IEEE, **1989**. p.91-100 of vi+398 pp. 9 refs. Conference: Ithaca, NY, USA, 7-9 Aug 1989

Abstract

Three key aspects of AlGaAs/InGaAs/GaAs MODFETs, namely current-handling capability, signal delay, and saturated output regime, are experimentally evaluated and correlated with the heterostructure configuration. Gate lengths down to 0.1 ***mu*** m and corresponding cutoff frequencies above 140 GHz are employed. The three aspects are found to be closely interrelated. By the incorporation of an InGaAs quantum well the two- ***dimensional*** -electron-gas (2DEG) density of the materials system can be considerably ***extended***. However, this results in only limited improvement for the ***FET*** current-handling capability above a 2DEG density of 2*1012 cm-2. The main effect on the MODFET current gain cutoff frequency is through the reduction of the input delay as demonstrated with 0.1- ***mu*** m-gate-length devices. Extracting the same intrinsic delay time means that the electron dynamics in the ***channel*** of AlGaAs/GaAs and pseudomorphic MODFETs is very comparable. This is consistent with the fact that there is no significant change in the effective electron mass, although changes in the intervalley scattering dynamics are still expected. Open-circuit voltage gain and output conductance are strongly related to the space-charge-layer configuration on top of the ***channel***. This is related to the ***recess*** configuration; however, for a large voltage gain a high structural aspect ratio is generally needed.

Controlled or Index Terms

ALUMINIUM COMPOUNDS; GALLIUM ARSENIDE; ***HIGH ELECTRON MOBILITY TRANSISTORS*** ; III-V SEMICONDUCTORS; INDIUM COMPOUNDS; SEMICONDUCTOR DEVICE TESTING

Supplementary Terms

gate length; intervalley scattering dynamics; open circuit voltage gain; MODFETs; current-handling capability; signal delay; saturated output regime;

heterostructure configuration; cutoff frequencies; InGaAs quantum well; 2DEG density; current gain cutoff frequency; electron dynamics; effective electron mass; output conductance; space-charge-layer configuration; ***recess configuration*** ; structural aspect ratio; ***0.1 micron*** ; 140 GHz; AlGaAs-InGaAs-GaAs CHI AlGaAs-InGaAs-GaAs int, AlGaAs int, InGaAs int, GaAs int, Al int, As int, Ga int, In int, AlGaAs ss, InGaAs ss, Al ss, As ss, Ga ss, In ss, GaAs bin, As bin, Ga bin PHP size 1.0E-07 m; frequency 1.4E+11 Hz ET As*Ga; As sy 2; sy 2; Ga sy 2; GaAs; Ga cp; cp; As cp; Al*As*Ga; Al sy 3; sy 3; As sy 3; Ga sy 3; AlGaAs; Al cp; As*Ga*In; In sy 3; InGaAs; In cp; V; Al*As*Ga*In; Al sy 4; sy 4; As sy 4; Ga sy 4; In sy 4; AlGaAs-InGaAs-GaAs; Al; As; Ga; In

☐ **L32 ANSWER 36 OF 46 INSPEC (C) 2004 IEE on STN DUPLICATE 9**

Accession Number

1988:3152239 INSPEC DN B88039451 Full Text

Title

Inverse-narrow-width effects and small-geometry MOSFET threshold voltage model.

Author/Inventor

Hsueh, K.K.-L.; Sanchez, J.L.; Demassa, T.A.; Akers, L.A.

Source

IEEE Transactions on Electron Devices (March **1988**) vol.35, no.3, p.325-38. 16 refs. Price: CCCC 0018-9383/88/0300-0325$01.00 CODEN: IETDAI ISSN: 0018-9383

Abstract

An analytical threshold voltage model is developed based on the results from a three-***dimensional*** ***MOSFET*** simulator, called MICROMOS. The model is derived by solving Poisson's equation analytically and is used to predict the threshold voltage of ***MOSFETs*** with fully ***recessed*** oxide isolation (the ***trench*** structure). Coupling was observed between the short-***channel*** effect and the inverse-narrow-***width*** effect. The coupling results from the mutual modulation of the depletion depth and is used to ***extend*** the analytical inverse narrow-***width*** model to small-geometry devices. The model is compared with experimental data obtained from the literature as well as with the three-***dimensional*** simulator. Satisfactory agreement for ***channel*** length down to 1.5 ***mu*** m and ***channel widths*** down to 1 ***mu*** m has been obtained.

Controlled or Index Terms

INSULATED GATE FIELD EFFECT TRANSISTORS ; SEMICONDUCTOR DEVICE MODELS

Supplementary Terms

small-geometry MOSFET ; threshold voltage model; ***three-dimensional MOSFET simulator*** ; MICROMOS; Poisson's equation; ***fully recessed oxide isolation*** ; ***trench structure*** ; ***short-channel effect*** ; ***inverse-narrow-width effect*** ; depletion depth; ***channel length*** ; ***channel widths*** ; ***1.5 micron*** ; ***1 micron*** PHP size 1.5E-06 m; size 1.0E-06 m

☐ **L32 ANSWER 37 OF 46 INSPEC (C) 2004 IEE on STN DUPLICATE 11**

Accession Number

1980:1446445 INSPEC DN B80004706 Full Text

Title

One-micrometer electron beam lithography FET technology.

Author/Inventor

Hunter, W.R.; Ephrath, L.M.; Grobman, W.; Osburn, C.M.; Crowder, B.L.; Cramer, A.; Luhn, H.E. (IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA)

Source

1978 International Electron Devices Meeting New York, NY, USA: IEEE, **1978**. p.54-7 of xxiv+687 pp. 11 refs. Washington, DC, USA, 4-6 Dec 1978 Sponsor(s): IEEE

Abstract

Describes the process technology used to fabricate high speed static and dynamic ***IGFET*** programmable logic array structures. An n- ***channel*** silicon gate technology, using electron-beam lithography with minimum ***dimensions*** of 1 ***mu*** m, was implemented. The six mask process employs semi-***recessed*** oxide isolation and makes extensive use of ion implantation, resist liftoff techniques and reactive ion etching (RIE). Implementation of a field ***etchback*** after source and drain implant to eliminate a low ***thick*** -oxide parasitic device threshold is also discussed.

Controlled or Index Terms

CELLULAR ARRAYS; ELECTRON BEAM LITHOGRAPHY; ***FIELD EFFECT*** INTEGRATED CIRCUITS; INTEGRATED CIRCUIT TECHNOLOGY; INTEGRATED LOGIC CIRCUITS

Supplementary Terms

electron beam lithography; ***IGFET programmable logic array*** ; ion implantation; resist liftoff techniques; reactive ion etching; ***field effect integrated circuits*** ; integrated logic circuits

☐ **L32 ANSWER 38 OF 46 INSPEC (C) 2004 IEE on STN**

Accession Number

2004:8058197 INSPEC DN B2004-09-2570D-024 Full Text

Title

35% drive current improvement from recessed -SiGe drain extensions on 37 nm gate length PMOS.

Author/Inventor

Chidambaram, P.R.; Smith, B.A.; Hall, L.H.; Bu, H.; Chakravarthi, S.; Kim, Y.; Samoilov, A.V.; Kim, A.T.; Jones, P.J.; Irwin, R.B.; Kim, M.J.; Rotondaro, A.L.P.; Machala, C.F.; Grider, D.T.

Source

2004 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.04CH37526) Gaithersburg, MD, USA: Widerkehr and Associates, 2004. p.48-9 of xiii+252 pp. 2 refs. Conference: Honolulu, HI, USA, 15-17 *June 2004* Price: CCCC 0-7803-8289-7/04/$20.00 ISBN: 0-7803-8289-7

Abstract

Results from the best reported PMOS transistor at a 37 ***nm*** gate length (Lg) built on a process with a ***recessed*** SiGe epitaxial layer are discussed. The process details include successful integration of SiGe at the drain ***extension*** (DE) location. A highly compressive SiGe layer, in close proximity to the ***channel*** , results in large hole mobility improvements. HRTEM based lattice parameter extractions confirm the compressive strain in the ***channel***. In situ doped B in SiGe can be activated to a higher degree than implanted B in bulk Si resulting in further improvements from the lower DE resistance. Both changes combine to give an unprecedented 35% PMOS performance improvement. Process and device simulations that predict the observed parametric behavior quantitatively isolate the improvements to be 28% from stress and 7% from DE resistance improvement.

Controlled or Index Terms

CMOS INTEGRATED CIRCUITS; GE-SI ALLOYS; ***MOSFET*** ; TRANSMISSION ELECTRON MICROSCOPY

Supplementary Terms

35% drive current improvement; ***recessed-SiGe drain extensions*** ; ***37 nm gate length PMOS*** ; large hole mobility; lattice parameter extractions; HRTEM; ***37 nm*** ; SiGe CHI SiGe int, Ge int, Si int, SiGe bin, Ge bin, Si bin PHP size 3.7E-08 m ET Ge*Si; Ge sy 2; sy 2; Si sy 2; SiGe; Si cp; cp; Ge cp; B; Si; Ge-Si; Ge

☐ **L32 ANSWER 39 OF 46 INSPEC (C) 2004 IEE on STN**

Accession Number

2003:7509322 INSPEC DN B2003-02-2560R-130 Full Text

Title

High performance damascene gate CMOSFETs with recessed channel formed by plasma oxidation and etching method (RC-POEM).

Author/Inventor

Matsuo, K.; Sekine, K.; Saito, T.; Nakajima, K.; Suguro, K.; Tsunashima, Y.

Source

International Electron Devices Meeting. Technical Digest (Cat. No.02CH37358) Piscataway, NJ, USA: IEEE, 2002. p.445-8 of 957 pp. 7 refs. Conference: San Francisco, CA, USA, 8-11 Dec **2002** Sponsor(s): Electron. Devices Soc. IEEE Price: CCCC 0-7803-7462-2/02/$17.00 ISBN: 0-7803-7462-2

Abstract

We report on high performance transistors using a new ***recessed channel*** formed by plasma oxidation and etching method (RC-POEM). The advantages of RC-POEM are: [a] lowering source/drain ***extension*** sheet resistance while suppressing lateral diffusion of ***extension*** region; [b] forming pseudo-raised ***extension*** using only plasma oxidation and wet etching. RC-POEM suppressed short ***channel*** effects down to 35nm physical gate length and high drive current were obtained.

Controlled or Index Terms

CAPACITANCE; DIFFUSION; ***MOSFET*** ; OXIDATION; SPUTTER ETCHING

Supplementary Terms

damascene gate CMOSFETs; ***recessed channel*** ; plasma oxidation; plasma etching method; RC-POEM; ***source/drain extension sheet resistance*** ; lateral diffusion; ***extension region*** ; ***pseudo-raised extension*** ; wet etching; ***short channel effects*** ; physical gate length; drive current; ***35 nm*** PHP size 3.5E-08 m

☐ **L32 ANSWER 40 OF 46 INSPEC (C) 2004 IEE on STN**

Accession Number

2001:6880678 INSPEC DN B2001-05-2560R-013 Full Text

Title

Analysis of a novel Elevated Source Drain MOSFET with reduced Gate-Induced Drain-Leakage current.

Author/Inventor

Kyung-Whan Kim; Chang-Soon Choi; Woo-Young Choi (Dept. of Electr. & Comput. Eng., Yonsei Univ., Seoul, South Korea)

Source

Proceedings 2000 IEEE Hong Kong Electron Devices Meeting (Cat. No.00TH8503) Piscataway, NJ, USA: IEEE, **2000**. p.36-9 of x+150 pp. 11 refs. Conference: Hong Kong, China, 24 June 2000 Sponsor(s): IEEE Electron Devices Soc.; Univ. Hong Kong Price: CCCC 0 7803 6304 3/2000/$10.00 ISBN: 0-7803-6304-3

Abstract

A new self-aligned ESD (Elevated Source Drain) ***MOSFET*** structure which can effectively reduce the GIDL (Gate-Induced Drain Leakage) current is proposed and analyzed. Proposed ESD structure is characterized by sidewall spacer ***width*** (WS) and ***recessed - channel*** depth (XR) which are determined by dry-etching process. Elevation of the Source/Drain ***extension*** region is realized so that the low-activation effect caused by low-energy ion implantation can be avoided. The GIDL current in the proposed ESD structure is reduced as the region with the peak electric field is shifted toward the drain side.

Controlled or Index Terms

LEAKAGE CURRENTS; ***MOSFET***

Supplementary Terms

gate-induced drain leakage current; ***self-aligned elevated source drain MOSFET*** ;

activation effect; ion implantation; dry etching; electric field

☐ **L32 ANSWER 41 OF 46 INSPEC (C) 2004 IEE on STN**

Accession Number

1994:4730581 INSPEC DN B9409-1350F-026 Full Text

Title

Very high voltage AlGaAs/InGaAs pseudomorphic power HEMTs.

Author/Inventor

Ming-Yih Kao; Shih-Tsang Fu; Pin Ho; Smith, P.M.; Chao, P.C.; Nordheden, K.J.; Sujane Wang (Electron Lab., Gen. Electr. Co., Syracuse, NY, USA)

Source

International Electron Devices Meeting 1992. Technical Digest (Cat. No.92CH3211-0) New York, NY, USA: IEEE, **1992**. p.319-21 of 1022 pp. 3 refs. Conference: San Francisco, CA, USA, 13-16 Dec 1992 Sponsor(s): Electron Devices Soc. IEEE Price: CCCC 0 7803 0817 4/92/$3.00 ISBN: 0-7803-0817-4

Abstract

This paper reports the development of double ***recessed*** pseudomorphic GaAs High Electron Mobility Transistors (***HEMTs***) for high voltage operation. The GaAs-based power ***HEMT*** with 0.25 ***mu*** m gate-length exhibited a gate to drain breakdown voltage of 30 volts, a peak gm of 510 mS/mm, and a maximum current density of 540 mA/mm. When biased to 14 volts on the drain, the 400 ***mu*** m wide ***HEMT*** delivered 505 mW (1.26 W/mm) output power at 4.5 GHz. This is the highest output power density and drain-source operating voltage ever reported for ***HEMT*** devices. The device also showed excellent 4.5 and 10 GHz power performance combination (power gain, power density, power-added efficiency) at Vds=8V. The significant ***extension*** of device drain bias range as well as increase in the product of current density and breakdown voltage were attributed to the adoption of ***channel recess*** using reactive ion etching.

Controlled or Index Terms

ALUMINIUM COMPOUNDS; GALLIUM ARSENIDE; ***HIGH ELECTRON MOBILITY TRANSISTORS*** ; III-V SEMICONDUCTORS; INDIUM COMPOUNDS; POWER TRANSISTORS; SEMICONDUCTOR TECHNOLOGY; SOLID-STATE MICROWAVE DEVICES; SPUTTER ETCHING

Supplementary Terms

pseudomorphic power HEMTs; double recessed transistors; high voltage operation; gate to drain breakdown voltage; peak transconductance; maximum current density; output power density; drain-source operating voltage; power gain; power density; power-added efficiency; drain bias range; breakdown voltage; ***channel recess*** ; reactive ion etching; ***0.25 micron*** ; 30 V; 505 mW; 4.5 GHz; 10 GHz; 14 V; 8 V; AlGaAs-InGaAs CHI AlGaAs-InGaAs int, AlGaAs int, InGaAs int, Al int, As int, Ga int, In int, AlGaAs ss, InGaAs ss, Al ss, As ss, Ga ss, In ss PHP size 2.5E-07 m; voltage 3.0E+01 V; power 5.05E-01 W; frequency 4.5E+09 Hz; frequency 1.0E+10 Hz; voltage 1.4E+01 V; voltage 8.0E+00 V ET Al*As*Ga; Al sy 3; sy 3; As sy 3; Ga sy 3; AlGaAs; Al cp; cp; Ga cp; As cp; As*Ga*In; In sy 3; InGaAs; In cp; As*Ga; As sy 2; sy 2; Ga sy 2; GaAs; V; Al*As*Ga*In; Al sy 4; sy 4; As sy 4; Ga sy 4; In sy 4; AlGaAs-InGaAs; Al; As; Ga; In

☐ **L32 ANSWER 42 OF 46 INSPEC (C) 2004 IEE on STN**

Accession Number

1992:4044977 INSPEC DN B9201-1350F-126 Full Text

Title

A submicron self-aligned gate GaAs MESFET processing technique for MMIC device fabrication.

Author/Inventor

Chen, C.Y.; Shieh, T.J.; Carter, R.L. (Dept. of Electr. Eng., Texas Univ.,

Arlington, TX, USA)

Source

Midcon/90. Conference Record Ventura, CA, USA: Electron. Conventions Manage, 1990. p.472-5 of xii+564 pp. 4 refs. Availability: Western Periodicals Co., 424 East Main Street, Ventura, CA 93001, USA Conference: Dallas, TX, USA, 11-13 Sept **1990** Sponsor(s): IEEE; ERA

Abstract

A self-aligned, ***recess*** -etched, T-gate (SART) processing technique is presented. It utilizes a ***channel recess*** and a gate ***undercut*** etch process to achieve a submicron gate length ***MESFET*** with a nominal 2 ***mu*** m drain-to-source spacing using the optical lithography technique. The process is effective for ***thin channel*** active layer devices and utilizes no sacrificial metal layer. It also offers process control for optimized gate-to-source spacing and gate length. The result of a SART ***MESFET*** with 75 ***mu*** m of gate ***width*** shows an MSG up to 17 dB and an fmax of 60 GHz.

Controlled or Index Terms

ETCHING; GALLIUM ARSENIDE; III-V SEMICONDUCTORS; MMIC; PHOTOLITHOGRAPHY; ***SCHOTTKY GATE FIELD EFFECT TRANSISTORS*** ; SOLID-STATE MICROWAVE DEVICES

Supplementary Terms

self-aligned recess-etched T-gate; channel recess; gate undercut etch process; submicron gate length; ***MESFET;*** drain-to-source spacing; optical lithography; active layer devices; process control; SART; 60 GHz; ***2 micron*** ; GaAs CHI GaAs int, As int, Ga int, GaAs bin, As bin, Ga bin PHP frequency 6.0E+10 Hz; size 2.0E-06 m ET As*Ga; As sy 2; sy 2; Ga sy 2; GaAs; Ga cp; cp; As cp; T; B; V; As; Ga

☐ **L32 ANSWER 43 OF 46 INSPEC (C) 2004 IEE on STN**

Accession Number

1985:2463195 INSPEC DN B85035163 Full Text

Title

Optimization of sidewall masked isolation process.

Author/Inventor

Teng, C.W.; Pollack, G.; Hunter, W.R. (Texas Instrum. Inc., Dallas, TX, USA)

Source

IEEE Transactions on Electron Devices (Feb. **1985**) vol.ED-32, no.2, p.124-31. 15 refs. Price: CCCC 0018-9383/85/0200-0124$01.00 CODEN: IETDAI ISSN: 0018-9383

Abstract

The authors present modifications of the sidewall masked isolation (SWAMI) process for VLSI device isolation which improve process reproducibility, eliminate stress-induced defects, and permit flexibility in ***channel*** stop implant optimization. A novel ***undercut*** -and-backfill technique is introduced to eliminate a localized failure mechanism of the oxidation mask by increasing the strength of the nitride-to-nitride joint. The primary variable influencing stress-induced defect generation is the vertical length of the sidewall nitride mask as determined by the amount of ***recessed*** silicon etch prior to sidewall nitride formation. In general, a maximum length can be found below which defect-free structures can be fabricated. An optional second ***recessed*** silicon etch, following the formation of the sidewall nitride, has been developed which increased the flexibility in optimizing the ***channel*** stop implantation. Defect-free low-leakage devices with near-zero electrical ***channel width*** reduction have been obtained.

Controlled or Index Terms

FIELD EFFECT INTEGRATED CIRCUITS; INTEGRATED CIRCUIT TECHNOLOGY; SEMICONDUCTOR TECHNOLOGY; VLSI

Supplementary Terms

MF3R; ***modified fully-framed-fully-recessed isolation*** ; sidewall masked isolation process; modifications; SWAMI; VLSI device isolation; process reproducibility; eliminate stress-induced defects; flexibility; ***channel stop implant*** ; optimization; ***novel undercut-and-backfill technique*** ; localized failure mechanism; oxidation mask; nitride-to-nitride joint; stress-induced defect generation; sidewall nitride mask; ***recessed silicon etch*** ; sidewall nitride formation; defect-free structures; ***second recessed silicon etch*** ; ***channel stop implantation*** ; low-leakage devices; ***near-zero electrical channel width reduction***

☐ **L32 ANSWER 44 OF 46 INSPEC (C) 2004 IEE on STN**

Accession Number

1984:2239749 INSPEC DN B84024981; C84023420 Full Text

Title

A three-dimensional simulation program for MOS devices and its application to the analysis of the narrow-channel effect.

Author/Inventor

Shigyo, N.; Konaka, M.; Dang, R. (Res. & Dev. Center, Toshiba Corp., Kawasaki, Japan)

Source

Transactions of the Institute of Electronics and Communication Engineers of Japan, Part C (Dec. **1983**) vol.J66C, no.12, p.1035-41. 21 refs. CODEN: DTGCAY ISSN: 0373-6113

Abstract

Describes a three-***dimensional*** device simulation program, TOPMOST, and its use in the analysis of the ***MOSFET*** narrow- ***channel*** effects. TOPMOST solves Poisson and current continuity equations by the finite-difference method and the box integration technique which has been ***extended*** to suit an arbitrary three-***dimensional*** structure. Using TOPMOST, it is shown that the 'inverse' narrow-***channel*** effect of a fully ***recessed*** field isolation structure can be suppressed by elevating the impurity level of the field region and/or tapering the side wall.

Controlled or Index Terms

DIGITAL SIMULATION; ELECTRONIC ENGINEERING COMPUTING; ***INSULATED GATE FIELD EFFECT TRANSISTORS***

Supplementary Terms

Poisson equations; ***three-dimensional simulation program*** ; TOPMOST; ***MOSFET*** ; ***narrow-channel effects*** ; current continuity equations; finite-difference method; box integration technique; ***three-dimensional structure*** ; ***fully recessed field isolation structure*** ; impurity level; tapering; side wall

☐ **L32 ANSWER 45 OF 46 COMPENDEX COPYRIGHT 2004 EEI on STN**

Accession Number

1986(5):68694 COMPENDEX DN *86106219; 860543016 Full Text

Title

ANALYSIS OF AN ANOMALOUS SUBTHRESHOLD CURRENT IN A FULLY RECESSED OXIDE MOSFET USING A THREE-DIMENSIONAL DEVICE SIMULATOR.

Author/Inventor

Shigyo, Naoyuki (Toshiba Corp, VLSI Research Cent, Kawasaki, Jpn); Dang, Ryo

Source

IEEE J Solid State Circuits v SC-20 n 1 Feb **1985** p 361-365 CODEN: IJSCBC ISSN: 0018-9200

Publication Year

1985

Abstract

A description is given of a three-***dimensional*** device simulator, TOPMOST, and of its use in the analysis of the anomalous subthreshold current hump in a fully ***recessed*** oxide MOS structure.TOPMOST solves the Poisson and current continuity equations using the finite-difference method and the box-integration technique, which has been ***extended*** to suit an arbitrary three-***dimensional*** structure.The device simulator can be optionally coupled with a two- ***dimensional*** process simulator for investigating the influence of process conditions on device performances.Using TOPMOST, the subthreshold current characteristics of a fully ***recessed*** oxide structure are examined.The mechanism underlying the hump is clarified, and the dependence on structure parameters, such as ***channel width*** , gate oxide ***thickness*** , and gate ***extension*** , is studied.It is shown that there is a worst case where the current hump becomes most conspicuous.It is also shown that the hump can be suppressed by a side-wall implantation.18 refs.

Controlled or Index Terms

*SEMICONDUCTOR DEVICES, ***MOSFET*** :Analysis; SEMICONDUCTOR MATERIALS:Analysis

Supplementary Terms

SUBTHRESHOLD CURRENTS; 3D DEVICE SIMULATORS; TOPMOST; ***RECESSED*** OXIDE STRUCTURES; CURRENT HUMPS

☐ **L32 ANSWER 46 OF 46 COMPENDEX COPYRIGHT 2004 EEI on STN**

Accession Number

1985(4):51110 COMPENDEX Full Text

Title

CONTROL OF THE GATE RECESS IN GaAs FET 's AND AlGaAs/GaAs TEGFET's PROCESS USING REACTIVE ION ETCHING.

Author/Inventor

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Source

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1984

Abstract

The authors report on the study of reactive ion etching of GaAs and Al0.3Ga0.7As using CCl2F2 and CF4 discharge. Selective etching of GaAs to AlGaAs, surface morphology and electrical characteristics of the etched materials are studied.The use of reactive ion etching for the controllable formation of ***channel*** layer in GaAs ***FET*** 's and AlGaAs/Gas Two-***Dimensional*** Electron Gas ***FET*** 's (TEGFET) and the possibility of adjusting their static characteristics after suitable annealing conditions are described.3 refs.

Controlled or Index Terms

*TRANSISTORS, ***FIELD EFFECT*** :Manufacture; SEMICONDUCTING GALLIUM ARSENIDE; SEMICONDUCTOR MATERIALS:Electric Properties; ETCHING:Applications

Supplementary Terms

EXTENDED ABSTRACT; ANNEALING TIME AND TEMPERATURE; SCHOTTKY DIODE FABRICATION; SEMICONDUCTOR MATERIAL DOPING ET As*Ga; As sy 2; sy 2; Ga sy 2; GaAs; Ga cp; cp; As cp; Al*As*Ga; Al sy 3; sy 3; As sy 3; Ga sy 3; Al0.3Ga0.7As; Al cp; C*Cl*F; CCl2F2; C cp; Cl cp; F cp; C*F; CF4; AlGaAs

☐ **L37 ANSWER 1 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2004-448194 [42] WPIX Full Text

Title

Manufacture of power semiconductor device, by implanting substrate with source dopant, reacting metal layer with substrate to form thin layer of highly conductive material on source regions, and forming contact mask on insulating layer.

Author/Inventor

DOLNY, G M; HAO, J; RIDLEY, R S

Patent Assignee/Corporate Source

(DOLN-I) DOLNY G M; (HAOJ-I) HAO J; (RIDL-I) RIDLEY R S

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2004104427	A1	20040603	(200442)*		8	H01L029-76

Priority Application Information

US 2001-44220	**20011120**
US 2003-618067	20030711

International Patent Classification

ICM H01L029-76
ICS H01L029-94

Abstract

US2004104427 A UPAB: 20040702
NOVELTY - Manufacture of power semiconductor device, comprises:
(i) implanting substrate with source dopant to form heavily doped source regions (114) in surface of semiconductor substrate;
(ii) depositing metal layer over substrate;
(iii) reacting metal layer with substrate to form ***thin*** layer of highly conductive material on source regions;
(iv) depositing layer of insulating on substrate; and
(v) forming contact mask of open and closed regions on insulating layer.
DETAILED DESCRIPTION - Manufacture of a power semiconductor device, comprises:
(a) forming a gate ***trench*** mask with open and closed regions on the surface of a semiconductor substrate;
(b) removing semiconductor material from areas exposed by the open regions of the ***trench*** mask to form gate ***trenches*** ;
(c) forming a gate oxide layer on the sidewalk of the ***trenches*** ;
(d) depositing a layer of conductive material on the surface of the substrate and in the ***trenches*** ;
(e) removing the conductive material from the surface of the semiconductor substrate and leaving enough conductive material in the ***trenches*** to fill the ***trenches*** ;
(f) implanting the substrate with a source dopant to form heavily doped source regions in the surface of the semiconductor substrate;
(g) depositing a metal layer over the substrate;
(h) reacting the metal layer with the substrate to form a ***thin*** layer of highly conductive material on the source regions;
(i) depositing a layer of insulating on the substrate;
(j) forming a contact mask of open and closed regions on the insulating layer and removing insulating material from open regions to expose portions of the surface having the highly conductive material on the source regions; and
(k) depositing and patterning a conductive layer over the surface of the

substrate to form electrical contacts to the highly conductive material on the source regions.

An INDEPENDENT CLAIM is also included for a power semiconductor device with ***trench*** gates, comprising:

(a) a semiconductor substrate;

(b) a source layer at one surface of the substrate and comprising a high concentration of a dopant of one polarity;

(c) a well layer beneath the source layer doped with a dopant of opposite polarity;

(d) ***trenches*** penetrating the source layer, the ***trenches*** filled with conductive material;

(e) a highly conductive layer on the surface of the source layer comprising a material reacted from a metal the semiconductor substrate;

(f) an insulating layer on the highly conductive layer;

(g) vias formed in the insulating layer and ***extending*** to the highly conductive layer on the source layer; and

(h) conductive material filling the vias for contacting the highly conductive layer.

USE - For manufacturing a power semiconductor device (claimed).

ADVANTAGE - Both the ***polysilicon*** (122) and BPSG ***recessed*** etches can be minimized, thus there is less defects and damage to each layer.

DESCRIPTION OF DRAWING(S) - The figure is a perspective partial sectional view of a power semiconductor device.

Source regions 114
P-well 120
Polysilicon 122
Via openings 160
Silicide 225
Dwg.9/9

Technology

US 2004104427 A1UPTX: 20040702 TECHNOLOGY FOCUS - METALLURGY - Preferred Component: The substrate comprises silicon and the metal deposited on the source regions is reacted with the substrate to form a ***silicide*** (225). The metal on the source regions is platinum or titanium. TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The insulating material is silicon dioxide and/or silicon nitride.

TECHNOLOGY FOCUS - CERAMICS AND GLASS - Preferred Material: The insulating material is borophosphosilicate glass (BPSG) and/or phosphosilicate glass.

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The device further comprises a drain layer on the other surface one surface of the substrate doped with a high concentration of a dopant of one polarity to form a power ***MOSFET***. The device further comprises a third layer beneath the well layer and comprising dopants of the one polarity and a cathode layer on the opposite surface of the substrate and highly doped with dopants of an opposite polarity to form a power thyristor.

Manual Codes

CPI: L04-C02B; L04-C05; L04-C06A; L04-C07E; L04-C10; L04-C10A; L04-C11C1; L04-C12; L04-C12A; L04-C12B; L04-C12C; L04-C12D EPI: U11-C02J6; U11-C05F1; U12-D02A

☐ **L37 ANSWER 2 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2004-020947 [02] WPIX Full Text

Title

Recessed channel complementary metal oxide semiconductor device comprises silicon-on-insulator layer having recessed channel region, and adjoining extension implant regions having abrupt lateral profile and are located below gate region.

Author/Inventor

DOKUMACI, O H; IEONG, M; KANARSKY, T S; KU, V

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2003189228	A1	20031009	(200402)*		10	H01L027-01
US 6677646	B2	20040113	(200405)			H01L027-01

Priority Application Information

US 2002-117959	20020405

International Patent Classification

ICM H01L027-01
ICS H01L027-12; H01L031-0392

Abstract

US2003189228 A UPAB: 20040702
NOVELTY - A ***recessed channel*** complementary metal oxide semiconductor (CMOS) device comprises a silicon-on-insulator (***SOI***) layer having a ***recessed channel*** region (24), and adjoining ***extension*** implant regions; and a gate region(s) present atop the ***SOI*** layer, where the adjoining ***extension*** implant regions have an abrupt lateral profile and are located below the gate region.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of fabricating a ***recessed channel*** CMOS device, comprising providing a patterned oxide layer over an ***SOI*** layer, the patterned oxide layer exposing a portion of the ***SOI*** layer; ***thinning*** the exposed region of the ***SOI*** layer to form a ***recessed channel*** region; forming a gate dielectric on the ***recessed channel*** region; forming sacrificial nitride spacers on portions of the gate dielectric to protect exposed walls of the ***SOI*** layer and the oxide layer, and forming a gate conductor on other portions of the gate dielectric not containing the sacrificial nitride spacers; ***recessing*** the oxide layer exposing ***SOI*** layer abutting the ***recessed channel*** region; forming source/drain diffusion regions in the exposed ***SOI*** layer abutting the ***recessed channel*** region; and removing the sacrificial nitride spacers and forming ***extension*** implant regions in the ***SOI*** layer, such that the ***extension*** implant regions have an abrupt lateral profile and are located below the gate conductor.

USE - Used as e.g. ***MOSFET*** for use in very large scale integration.

ADVANTAGE - The invention is of high-performance, and has minimized short-***channel*** effect and series resistance. Its external resistance is not degraded.

DESCRIPTION OF DRAWING(S) - The figure is a pictorial representation illustrating the formation of the ***recessed channel*** CMOS device.

Bottom silicon-containing layer 10
Insulating layer 12
Top silicon-containing layer 14
Trench isolation regions 18
Recessed channel region 24 Dwg.6/12

Technology

US 2003189228 A1UPTX: 20040107 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The ***SOI*** layer is part of an ***SOI*** structure. It comprises source/drain regions. The gate region comprises a gate dielectric and a gate conductor. The ***recessed channel*** CMOS comprises halo implant regions that have an abrupt lateral profile, which are located below the gate region; and

permanent spacers present on exposed sidewalls of the gate region. Preferred ***Dimension*** : The ***recessed channel*** region has a ***thickness*** of 5-20 ***nm***. Preferred Method: ***Thinning*** is carried out by chemical downstream etching, reactive-ion etching, or thermal oxidation and etching. It is carried out by thermal oxidation and a chemical oxide removal (COR) process. Source/drain ***extension*** and halo implant regions are formed by angled implantation and annealing. Halo implant regions are formed after forming the ***extension*** implant regions. Preferred Condition: COR process is carried out at relatively low pressures of at most6 mtorr, and in a vapor of hydrofluoric acid and ammonia.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Component: The gate dielectric comprises silicon dioxide, silicon nitride, silicon oxynitride, titanium dioxide, aluminum oxide, zirconium oxide, tantalum oxide, and/or lanthanum oxide.

TECHNOLOGY FOCUS - METALLURGY - Preferred Component: The gate conductor comprises ***polysilicon*** , an elemental conductive metal, an alloy that includes an elemental conductive metal(s), a ***silicide*** of an elemental conductive metal, and/or a nitride of an elemental conductive metal.

Manual Codes

CPI: L04-C02B; L04-C11C1; L04-C12A; L04-C12B; L04-E01B1 EPI: U13-D02A; U13-D07

☐ **L37 ANSWER 3 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-626459 [59] WPIX Full Text

Title

Semiconductor device, e.g. metal oxide semiconductor field effect transistor, comprises metal gate electrode surrounded by polysilicon layers and gate oxide film whose edges are thicker than its center portion.

Author/Inventor

KWON, H Y

Patent Assignee/Corporate Source

(HYUN-N) HYUNDAI ELECTRONICS IND CO LTD; (HYNI-N) HYNIX SEMICONDUCTOR INC; (KWON-I) KWON H Y

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2003122202	A1	20030703	(200359)*		10	H01L029-76
JP 2003289143	A	20031010	(200367)		7	H01L029-78
KR 2003058641	A	20030707	(200377)			H01L021-334

Application Details

US 2003122202 A1 US 2002-329680 **20021227**

International Patent Classification

ICM H01L021-334; H01L029-76; H01L029-78
ICS H01L021-28; H01L029-423; H01L029-49

Abstract

US2003122202 A UPAB: 20030915
NOVELTY - Semiconductor device, e.g. metal ***oxide*** semiconductor ***field effect*** transistor, comprises a metal gate electrode surrounded by ***polysilicon*** layers and a gate oxide film whose edges are ***thicker*** than its center portion formed by a thermal oxidation process.

DETAILED DESCRIPTION - Semiconductor device comprises:

(a) a semiconductor substrate (31) having a ***channel*** region and an impurity region disposed at both sides of the ***channel*** region;

(b) a first ***polysilicon*** layer (35) disposed on a surface of the ***channel***

region;

(c) a gate oxide film (33) disposed between the first ***polysilicon*** layer and the surface of the ***channel*** region and ***extending*** laterally to have a ***width*** larger than that of the first ***polysilicon*** film, where a ***thickness*** of the edge of the gate oxide film is larger than that of its center portion to surround side walls of the first ***polysilicon*** film;

(d) a gate electrode disposed on the first ***polysilicon*** film and comprising a metal layer and a second ***polysilicon*** layer surrounding the metal layer; and

(e) an insulating film spacer disposed on both sides of the gate electrode.

An INDEPENDENT CLAIM is also included for a method for manufacturing a semiconductor device, which comprises:

(1) providing a semiconductor substrate having an element isolating film (32) defining an active region;

(2) forming a dummy gate comprising a gate oxide film, a first ***polysilicon*** layer and a hard mask layer sequentially stacked on the active region;

(3) performing a thermal oxidation process to the overall surface to form a thermal oxide film on the sidewalls of the first ***polysilicon*** layer and on both sides of the gate oxide film, where the thermal oxidation film on both sides of the gate oxide film is ***thicker*** than the gate oxide film;

(4) forming a low concentration impurity region by performing a first ion implantation process on the entire surface including the dummy gate;

(5) forming an insulating film over the resulting structure;

(6) ***etching back*** the insulating film and the thermal oxide film on the semiconductor substrate to form an insulating film spacer on the sidewall of the dummy gate;

(7) forming a high concentration impurity region in the semiconductor substrate on both sides of the dummy gate electrode by performing a second ion implantation process;

(8) forming a planarized interlayer insulating film for exposing the upper portion of the dummy gate;

(9) removing the hard mask layer to form ***groove*** exposing the first ***polysilicon*** layer;

(10) forming a Vth ion implantation region in a ***channel*** region of the semiconductor substrate by performing a third ion implantation process;

(11) subjecting the resultant structure to a thermal annealing process;

(12) sequentially forming a second ***polysilicon*** layer on the entire surface and a metal layer filling the ***groove*** ;

(13) ***etching back*** the metal layer to form a ***recessed*** metal pattern in the ***groove*** ;

(14) forming a third ***polysilicon*** layer overall surface of the resulting structure to fill the ***recess*** region in the ***groove*** ; and

(15) planarizing the resultant to expose the interlayer insulating film.

USE - Used as semiconductor device e.g. ***MOSFET***.

ADVANTAGE - The source/drain region does not overlap when the ion implantation process is performed for forming the Vth ion implantation region because the gate oxide film whose edge is ***thicker*** than its center portion is employed resulting in decrease of electric field value and reduced junction capacitance so improving reliability on hot carrier. The process employs a conventional ***MOSFET*** manufacturing process which reduces resistance of the source/drain region and prevents damage due to the gate etching process.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section of a semiconductor device during manufacture.

Semiconductor substrate 31

Element isolating film 32

Gate oxide film 33

Polysilicon layer 35

Dwg.2a/2

Technology

US 2003122202 A1UPTX: 20030915 TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The gate oxide film is a thermal oxide film including silicon dioxide, silicon nitride or tantalum oxide. The metal layer comprises tungsten or aluminum.

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The impurity region comprises a low concentration impurity region ***extending*** from both ends of the ***channel*** region ***extending*** from both sides of the low concentration impurity region. The low and high concentration impurity regions are ion implanted having a first conductive type, and the ***channel*** region is ion-implanted with an ion having a second conductivity type opposite to the first.

Manual Codes

CPI: L04-C10B; L04-C11C1; L04-C12A; L04-E01B1 EPI: U11-C18A3; U12-D02A

☐ **L37 ANSWER 4 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-266650 [26] WPIX Full Text

Title

Dual gate logic device, e.g. metal oxide semiconductor field effect transistor, includes substrate having major lateral surface, with fourth region partially overlapping second region, and third region partially overlapping first region.

Author/Inventor

FURUKAWA, T; HAKEY, M C; HOLMES, S J; HORAK, D V; MA, W H; HAKEY, M; HOLMES, S; HORAK, D; MA, W

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM UK LTD

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2002187610	A1	20021212	(200326)*		25	H01L021-336
WO 2002101834	A2	20021219	(200326)	EN		H01L029-49
US 6596597	B2	20030722	(200354)			H01L021-336
EP 1396029	A2	20040310	(200418)	EN		H01L029-49
TW 564468	A	20031201	(200431)			H01L021-00
KR 2004006032	A	20040116	(200434)			H01L029-49
AU 2002310613	A1	20021223	(200452)			H01L029-49

International Patent Classification

ICM H01L021-00; H01L021-336; H01L029-49
ICS H01L021-28; H01L021-8238; H01L029-786

Abstract

US2002187610 A UPAB: 20040813
NOVELTY - A dual gate logic device comprises a silicon substrate having a major lateral surface, a first layer comprising first and second regions, and a second layer comprising third and fourth regions. The fourth region partially overlaps the second region, and the third region partially overlaps the first region.

DETAILED DESCRIPTION - A dual gate logic device comprises a silicon substrate having a major lateral surface, a first layer comprising first and second regions, and a second layer comprising third and fourth regions.

The first region comprises a dielectric fill material; and the second region sequentially comprises a first insulator stratum (11), a first germanium-containing gate conductor stratum (32), a gate dielectric stratum (22), and a single-crystal silicon stratum. The first and second regions reside on the major lateral surface.

The third region comprises a second dielectric fill material; and the fourth region comprises a second gate dielectric stratum, a second germanium-containing gate conductor stratum (32a), and a second insulating stratum (120).

The fourth region partially overlaps the second region, and the third region partially overlaps the first region.

An INDEPENDENT CLAIM is also included for a method for forming a an intermediary structure for use in a dual gate device, comprising:

(i) providing a single-crystal silicon substrate;

(ii) conformally applying a dielectric coating on an exterior sidewalls and the top surface of the pillars and remaining upper surfaces of the single-crystal silicon substrate;

(iii) covering the conformal dielectric coating with a dielectric fill to a height at least of the dielectric coating on the top surface of the pillar;

(iv) removing the dielectric coating to create a new top surface of the pillar and planarizing the dielectric fill to the new pillar top surface;

(v) applying a silicon wafer to the planarized dielectric fill surface and the new pillar top surface; and

(vi) etching the lower single-crystal silicon surface to a depth of the conformal dielectric coating on the single crystal silicon upper surface, the conformal coating acting as an etch stop thus creating isolated single-crystal ***channels***.

USE - As a dual gate logic device, e.g. ***MOSFET***.

ADVANTAGE - The method provides a self-aligned gate conductors and ***channels*** that are of constant ***width*** , thus preventing device yield and performance contriction.

DESCRIPTION OF DRAWING(S) - The figure shows the method.

First insulator stratum 11

Gate dielectric stratum 22

Germanium-containing gate conductor stratum 32

Germanium-containing gate conductor stratum 32a

Void region 46a

Second insulating stratum 120

Dwg.1/2

Technology

US 2002187610 A1UPTX: 20030428 TECHNOLOGY FOCUS - ELECTRONICS - Preferred ***Dimension*** : The single-crystal silicon region is approximately300-1000Angstrom ***thick***. The germanium-containing region is approximately0.05-0.3 ***mum thick***. Preferred Component: A composite pillar is disposed on the major lateral surface comprising sequentially, a first insulating region, a first germanium-containing region having a cross-sectional area and an exterior surface, a first gate dielectric region, a single-crystal silicon region having a cross-sectional area, and a second gate dielectric layer, a second germanium-containing gate conductor region, and a second insulating region. A laminate region(s) is disposed on the major lateral surface, comprising sequentially a first dielectric insulation fill stratum, and a second dielectric insulation fill stratum. The composite pillar and the laminate region are separated by a ***void*** region (46a). Preferred Method: ***Recessing*** is performed by isotropic etching accomplished with CF2C12 at 100 mtorr and 500-1500 watts. The germanium-gate exterior surfaces are thermally oxidized at 550degreesC, 0.5-0.7 torr oxygen, and 10-150 V bias on the substrate.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The substrate comprises a single-crystal silicon. The first and second germanium-containing gate conductor comprises at most50% silicon. The first and second insulation regions comprise silicon oxide, silicon nitride, or aluminum oxide. The dielectric coating comprises germanium nitride, germanium oxynitride germanium oxide, silicon dioxide, silicon nitride, hafnium oxide, aluminum oxide, tantalum

oxide, or titanium oxide. The ***void*** is filled with ***polysilicon*** filler doped with nitrogen or phosphorus dopants comprising diborane, arsine, and phosphine. at 1x1019-1x1021 atoms/cm2.

Manual Codes

CPI: L04-E01B1; L04-E06 EPI: U11-C05B9A; U11-C07C1; U11-C18A3; U12-D02A9; U13-D02

☐ **L37 ANSWER 5 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2003-029314 [02] WPIX Full Text

Title

Field effect transistor for integrated circuits, includes polysilicon gate regions having silicide sidewalls recessed from source and drain regions.

Author/Inventor

ADKISSON, JW; AGNELLO, PD; BALLANTINE, AW; DIVAKARUNI, R; JONES, EC; RANKIN, JH

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2002140039	A1	20021003	(200302)*		10	H01L029-76

International Patent Classification

ICM H01L029-76

Abstract

US2002140039 A UPAB: 20030204

NOVELTY - A ***field effect*** transistor comprises a conduction ***channel*** of sub-lithographic ***width*** ; source and drain regions having ***silicide*** sidewalls; and ***polysilicon*** gate regions on opposing sides of the conduction ***channel***. The ***polysilicon*** has ***silicide*** sidewalls and is ***recessed*** from the source and drain regions.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a method of forming the inventive ***field effect*** transistor. The method involves depositing regions of pad nitride on a silicon layer; etching the silicon layer to ***undercut*** the pad nitride to form a conduction ***channel*** between a source region and a drain region; depositing ***polysilicon*** to the portion where the silicon has been etched; etching through the ***polysilicon*** ; depositing ***silicide*** on remaining ***polysilicon*** and silicon; and removing the ***silicide*** and ***polysilicon*** from sides of the conduction ***channel*** near the source and drain regions.

USE - For use as ***field effect*** transistor for integrated circuits.

ADVANTAGE - The inventive ***field effect*** transistor has gate, source and drain with low resistivity achieved by the ***silicide*** sidewalls. The transistor has also low gate-to-junction capacitance achieved by ***recessing*** the ***silicide*** and ***polysilicon*** dual gate structure from the source and drain region edges.

DESCRIPTION OF DRAWING(S) - The figure shows the ***field effect*** transistor. Dwg.5/5

Technology

US 2002140039 A1UPTX: 20030111 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The ***silicide*** sidewalls maybe in the form of a liner. The ***polysilicon*** regions are connected by a damascene connector which is formed in a ***trench*** in at least one of an isolation structure or a pad material ***extending*** over an edge of the ***polysilicon*** gate regions. Preferred Method: The ***silicide*** deposition step includes depositing a disposable hard mask to define the active area of the transistor. The method further includes stripping the disposable hard mask; depositing a conformal layer of ***polysilicon*** and ***silicide*** ; applying a further mask; and etching ***silicide*** and ***polysilicon*** in accordance with the further mask.

TECHNOLOGY FOCUS - CERAMICS AND GLASS - Preferred Material: The disposable hard mask is borosilicate glass, doped glass or arsenic doped glass, or ozone tetraethylorthosilicate.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The ***silicide*** of the conformal layer consists of tungsten, cobalt or titanium ***silicides***.

Manual Codes

CPI: L04-C07; L04-C10B; L04-C10F; L04-E01B1 EPI: U11-C18A3; U12-D02A

☐ **L37 ANSWER 6 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2002-557191 [59] WPIX Full Text

Title

Vertical double-diffused insulated gate transistor includes conductive gate having high conductivity metal coextensive with polysilicon layer.

Author/Inventor

MEYER, T O; MOSIER, J W; PIKE, D A; TSANG, D W

Patent Assignee/Corporate Source

(ADPO-N) ADVANCED POWER TECHNOLOGY INC

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2002074585	A1	20020620	(200259)*		14	H01L029-74

International Patent Classification

ICM H01L029-74
ICS H01L031-111

Abstract

US2002074585 A UPAB: 20020916

NOVELTY - A vertical double-diffused insulated gate transistor comprises conductive gate having high conductivity metal coextensive with ***polysilicon*** layer.

DETAILED DESCRIPTION - A vertical double-diffused insulated gate transistor comprises a silicon substrate (20) with doping of a first dopant type, a gate oxide layer disposed over the substrate surface, a gate conductive layer on the gate oxide layer, a double-diffused dopant region of opposite two types of dopant types disposed within the substrate to define two PN junctions spaced laterally apart under the gate oxide layer and contoured in accordance with the defined outline characteristics, and a source conductive layer on the upper substrate surface and contacting the source region within an opening. The source conductive layer is spaced apart and electrically separate from the conductive layer. The gate conductive layer (60) comprises doped ***polysilicon*** (62) on the gate oxide layer and a metal layer coextending on the doped ***polysilicon***. It collectively defines the opening of a defined outlined characteristics. The PN junctions define portions of a ***field effect*** transistor. The portions include a source region (86) of a first type dopant in the substrate adjacent the outline characteristic and bounded by the first PN junction, a drain region of the first dopant type bounded by the second PN junction and spaced laterally from the outline characteristics and ***extending*** downwardly into the substrate, and a body region (90) of the second dopant type ***extending*** between the two PN junctions with a ***channel*** portion underlying the gate oxide layer and gate conductive layer. The ***channel*** portion is operable under ***field effect*** to conduct current between the source and drain regions.

USE - As vertical double-diffused insulated gate insulator, e.g. power metal ***oxide*** semiconductor (***MOS***) ***field - effect*** devices including power ***MOS***

field - effect transistors, ***insulated*** gate bipolar transistor, and MOS controlled thyristor.

ADVANTAGE - The invention avoids the uncertainties and difficulties of photolithography and localized oxidation of silicon layer formation in forming the functional areas of ***recessed*** gate ***field effect*** power metal ***oxide*** semiconductor (MOS) device. It facilitates P-body and N-source shorting without having to trade off series source resistance against vertical ***channel*** resistance in a ***recessed*** gate ***field effect*** power ***MOS*** device. It increases the yield of functional ***recessed*** gate ***field effect*** power ***MOS*** device. It has an improved ruggedness and an effective doubling of ***channel width*** over the prior art.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a portion of a silicon substrate.

Silicon substrate 20
Sidewall spacers 44
Gate conductive layer 60
Polysilicon 62 Source region 86
Body region 90
Metallization 94, 98
Dwg.12/25

Technology

US 2002074585 A1UPTX: 20020916 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: Insulative sidewall spacers (44) are disposed along the defined outline characteristic, and laterally separate the gate conductive layer and source conductive layer. A low-resistivity contact layer is included between the source region and the source conductive layer. The metal layer of the gate conductive layer is aligned with the doped ***polysilicon*** between the spacers. A dielectric layer is disposed over the gate conductive layer. Metallization (94, 98) is disposed on the dielectric layer and contacting the gate conductive layer through the openings in the dielectric layers.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Component: The source conductive layer comprises aluminum. The metal layer of the gate conductive layer comprises aluminum. The dielectric layer comprises oxide, nitride, oxy-nitride, glass and/or phosphosilicate glass.

Manual Codes

CPI: L04-E01B1 EPI: U11-C18A3; U12-D02A; V05-M

☐ **L37 ANSWER 8 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2002-488204 [52] WPIX Full Text

Title

Dynamic random access memory cells comprise silicon epitaxial layer over an insulating layer.

Author/Inventor

CHA, R C L; CHAN, L; TEE, K C

Patent Assignee/Corporate Source

(CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 6384437	B1	20020507	(200252)*		9	H01L027-148

International Patent Classification ICM H01L027-148

Abstract

US 6384437 B UPAB: 20020815

NOVELTY - Dynamic random access memory (DRAM) cells comprise silicon epitaxial layer (18) over an insulating layer.

DETAILED DESCRIPTION - DRAM cells comprise (i) a shallow ***trench*** isolation around device areas having ***recesses*** over and aligned to the device areas; (ii) an insulating layer (12) on a substrate (10) in the ***recesses*** having an opening in the insulating layer to the substrate; (iii) an epitaxial layer in each of the ***recesses*** ***extending*** from the opening and laterally over the insulating layer; (iv) a gate oxide on the epitaxial layer in each of the ***recesses*** ; (v) ***field*** ***effect*** transistors gate electrodes (22A) on the gate oxide and over the openings in the insulating layer having lightly doped source/drain areas and source/drain contact areas in the epitaxial layer adjacent to the gate electrodes; (vi) capacitor node contacts (28) to the source/drain contact areas in the epitaxial layer over the insulating layer; (vii) bit line contacts in the epitaxial layer over the insulating layer; and (viii) capacitors over and contacting the capacitor node contacts, and bit lines (36) over and contacting the bit line contacts.

USE - For DRAM devices.

ADVANTAGE - The invention has increased cell density while reducing the capacitor leakage current and has improved DRAM device performance.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-sectional view of memory cells. substrate 10

insulating layer 12

epitaxial layer 18

field ***effect*** transistors gate electrodes 22A

capacitor node contacts 28

bit lines 36

Dwg.10/10

Technology

US 6384437 B1 UPTX: 20020815 TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Components: The semiconductor substrate is a P-doped single-crystal Si substrate. The insulating layer is a silicon oxide (SiO) having a ***thickness*** of 100-200 ***Angstrom***. The epitaxial layer is single-crystal Si having a ***thickness*** of 1000-5000 ***Angstrom***. The gate oxide is SiO having a ***thickness*** of 15-35 ***Angstrom***. The gate electrodes are conductively doped ***polysilicon***.

Manual Codes

CPI: L03-G04A; L04-C12A; L04-C14A EPI: U11-C05B5; U11-C05F1; U11-C05G1B; U11-C08A3; U11-C08C; U11-C18A3; U12-C02A1; U13-C04B1A; U14-A03B4

☐ **L37 ANSWER 9 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2002-415213 [44] WPIX Full Text

Title

Fabrication of dynamic random access memory cells involves the use of selective silicon epitaxial growth over insulating layer on the cell areas.

Author/Inventor

CHA, R C L; CHAN, L; TEE, K C

Patent Assignee/Corporate Source

(CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 2002052077	A1	20020502	(200244)*		11	H01L021-8242

International Patent Classification ICM H01L021-8242

Abstract

US2002052077 A UPAB: 20020820

NOVELTY - Dynamic random access memory cells are fabricated by using selective silicon epitaxial growth over an insulating layer on the cell areas.

DETAILED DESCRIPTION - Fabrication of dynamic random access memory (DRAM) cells on and in an epitaxial silicon layer formed over a first insulating layer on a semiconductor substrate involves forming the first insulating layer on the substrate; depositing a hard-mask layer on the first insulating layer; patterning the hard-mask layer and leaving portions over device areas, and using the hard mask for etching shallow ***trenches*** in the substrate; depositing a second insulating layer to fill the shallow ***trenches*** and polishing back to the hard-mask layer to form shallow ***trench*** isolation; selectively removing the hard-mask layer and forming ***recesses*** over and self-aligned to the device areas and exposing the first insulating layer in the ***recesses*** ; etching openings in the first insulating layer over the device areas to the substrate; growing selectively the epitaxial layer from the openings and ***extending*** laterally over the first insulating layer in the ***recesses*** ; forming a gate oxide on the epitaxial layer; forming a doped ***polysilicon*** layer on the substrate; patterning the ***polysilicon*** layer to form ***field effect*** transistor (***FET***) gate electrodes over the openings, and implanting to form first and second source/drain contact areas in the epitaxial layer adjacent to the gate electrodes; forming insulating sidewall spacers on the gate electrodes, and implanting to form first and second source/drain contact areas adjacent to the sidewall spacers; and forming capacitors electrically contacting the first source/drain contact areas and bit lines electrically contacting the second source/drain contact areas to complete the DRAM cells.

USE - The method is used for fabricating DRAM cells. It is particularly useful for reducing capacitor leakage currents and soft error due to Alpha particles on DRAM cells. The DRAM cell produced can also be used for transistors to reduce leakage current.

ADVANTAGE - The inventive method provides DRAM cells with increased cell density while reducing capacitor leakage currents. It minimizes manufacturing costs of current DRAM process by integrating the selective silicon epitaxy on insulator without increasing the processing steps. Dwg.0/10

Technology

US 2002052077 A1UPTX: 20020711 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The first insulating layer is silicon oxide formed by thermal oxidation to a ***thickness*** of 100-200 ***Angstrom***. The hard-mask layer is silicon nitride deposited by low-pressure chemical vapor deposition to a ***thickness*** of 1600-2000 ***Angstrom***. The shallow ***trenches*** are etched to a depth of 2000-3300 ***Angstrom***. The second insulating layer is silicon oxide deposited by low pressure chemical vapor deposition and is polished back to form a field oxide, which is coplanar with top surface of the hard mask. The epitaxial layer is formed in a reactor using a reactant gas including silane (SiH4) or dichlorosilane (SiH2Cl2) at 950-1100degreesC, and the epitaxial layer is formed to a ***thickness*** of 1000-5000 ***Angstrom***. The gate oxide is formed by a dry thermal oxidation and is grown to a ***thickness*** of 15-35 ***Angstrom*** . The doped ***polysilicon*** layer is deposited by low-pressure chemical vapor deposition using a reactant gas of SiH4 and is doped N+ by ion implantation to a final concentration to a final concentration of 1x1019 to 4x1021 atoms/cm3. The method may include depositing a first interpolysilicon oxide (IPO1) layer (26) and etching first contact openings to the first source/drain contact areas and forming stacked capacitors having node contacts in the first contact openings; and depositing a second interpolysilicon oxide (IPO2) layer (32) and etching second contact openings to the second source/drain contact areas and forming bit line contact plugs in the second contact openings and forming bit lines to complete the DRAM cells. The IPO1 layer is silicon oxide deposited by chemical vapor deposition and planarized to a ***thickness*** to insulate the gate electrodes. The node contacts are formed from an N+ doped ***polysilicon***. The IPO2 layer is silicon oxide deposited by chemical

vapor deposition and planarized to a ***thickness*** to insulate the capacitors.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The substrate is a P doped single-crystal silicon substrate. The sidewall spacers are silicon oxide/silicon nitride. The gate electrodes are conductively doped ***polysilicon***. The node contacts (28) are formed from an N+ doped ***polysilicon***.

Manual Codes

CPI: L04-C01B EPI: U11-A01; U12-E01; U14-C01

☐ **L37 ANSWER 10 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2002-088901 [12] WPIX Full Text

Title

Fabrication of dynamic random access memory cells involves forming first insulating layer useful as stress-release layer for hard mask layer, and forming epitaxial layer over first insulating layer.

Author/Inventor

CHA, R C L; CHAN, L; KHENG-CHOK, T; RANDALL CHER LIANG, C; TEE, K C

Patent Assignee/Corporate Source

(CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 6319772	B1	20011120	(200212)*		10	H01L021-8242
SG 88834	A1	20020521	(200247)			H01L021-8242
SG 99375	A1	20031027	(200377)			H01L000-00

International Patent Classification ICM H01L000-00; H01L021-8242

Abstract

US 6319772 B UPAB: 20031128

NOVELTY - Dynamic random access memory (DRAM) cells are fabricated by forming first insulating layer, patterning hard mask layer, etching shallow ***trenches*** , forming shallow ***trench*** isolation, removing hard mask layer, etching openings, growing epitaxial layer which ***extends*** over insulating layer in ***recesses*** , and forming ***field effect*** transistor and DRAM capacitors on epitaxial layer after growing gate oxide.

DETAILED DESCRIPTION - Fabrication of DRAM cells in an epitaxial silicon layer on semiconductor substrate (10) includes forming a first insulating layer (12) on the substrate and depositing a hard mask layer on the first insulating layer. The hard mask layer is patterned to leave portions over device areas. Shallow ***trenches*** are etched in the substrate using the hard mask. A second insulating layer (16) is deposited to fill the shallow ***trenches*** and is polished back to the hard mask layer to form shallow ***trench*** isolation. The hard mask is removed to form ***recesses*** over and self-aligned to the device areas exposing the first insulating layer. Openings are etched in the first insulating layer over device areas to the substrate. An epitaxial layer is grown from the openings and ***extends*** laterally over the first insulating layer in the ***recesses***. A gate oxide is formed on the epitaxial layer and a doped ***polysilicon*** layer is formed on the substrate. ***Field effect*** transistor gate electrodes (22A) are formed over the openings by patterning the ***polysilicon*** layer, and lightly-doped source/drain areas are formed in the epitaxial layer adjacent to the gate electrodes. Insulating sidewall spacers (24) and first and second source/drain contact areas (19N+) are formed on the gate electrodes. Capacitors are formed to electrically contact the first source/drain contact areas, and bit lines are formed to electrically contact the second source/drain areas.

USE - None given.

ADVANTAGE - The method reduces capacitor leakage current and improves DRAM cell performance. It increases memory cell density and can be integrated into current DRAM processes to reduce cost.

DESCRIPTION OF DRAWING(S) - The figure shows cross-sectional view of the DRAM cell.

Substrate 10

First insulating layer 12

Second insulating layer 16

First and second source/drain contact areas 19+

Field effect transistor gate electrodes 22A

Sidewall spacers 24

Dwg.9/10

Technology

US 6319772 B1 UPTX: 20020221 TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The semiconductor substrate is P-doped single-crystal silicon substrate. The first insulating layer having a ***thickness*** of 100-200Angstrom comprises silicon oxide formed by thermal oxidation. The hard-mask layer having a ***thickness*** of 1600-2000Angstrom comprises silicon nitride formed by low-pressure chemical vapor deposition (LPCVD). The shallow ***trenches*** are etched to a depth of 2000-3300Angstrom. The second insulating layer comprises silicon oxide deposited by LPCVD. The epitaxial layer having a ***thickness*** of 1000-5000Angstrom is formed in a reactor using silane and/or dichlorosilane at 950-1100degreesC. The gate oxide having a ***thickness*** of 15-35Angstrom is formed by dry thermal oxidation. The doped ***polysilicon*** layer is formed by LPCVD using silane and is N+ doped by ion implantation to a final concentration of 1x1019 - 4x1021 atoms/cm3. The sidewall spacers are silicon oxide/silicon nitride.

Manual Codes

CPI: L03-G04A; L04-C01; L04-C06; L04-C06A; L04-C07E; L04-C10B; L04-C11C1; L04-C12; L04-C12A; L04-C12C EPI: U11-C18B5; U13-C04B1A; U14-A03B4

☐ **L37 ANSWER 14 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2000-441756 [38] WPIX Full Text

Title

Microelectronic structure e.g., field effect transistor has a substrate having a top surface defining a first plane, a dielectric, a gate electrode, and source and drain terminals.

Author/Inventor

CHAU, R S; JAN, C; MORROW, P; MURTHY, A S; PACKAN, P

Patent Assignee/Corporate Source

(ITLC) INTEL CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
WO 2000030169	A1	20000525	(200038)*	EN	29	H01L021-336
AU 2000014702	A	20000605	(200042)			H01L021-336
EP 1147552	A1	20011024	(200171)	EN		H01L021-336
KR 2001080432	A	20010822	(200213)			H01L021-336
JP 2002530864	W	20020917	(200276)		28	H01L029-78

Priority Application Information

US 1998-191076	19981112

International Patent Classification ICM H01L021-336; H01L029-78

Abstract

WO 200030169 A UPAB: 20000811

NOVELTY - A microelectronic structure comprises a substrate having a top surface

that defines a first plane; a dielectric disposed superjacent the top surface of the substrate; a gate electrode disposed superjacent the dielectric; and a source terminal and a drain terminal each disposed and adjacent one of the first side wall spacers partially within the substrate and partially above the substrate.

DETAILED DESCRIPTION - A microelectronic structure comprises a substrate having a top surface that defines a first plane; a dielectric (104) disposed superjacent the top surface of the substrate (102); a gate electrode (106) disposed superjacent the dielectric; and source and drain terminals (110) each disposed and adjacent to one of the first side wall spacers partially within and/or above the substrate. The source and drain terminals have a portion that ***extends*** laterally so as to be subjacent at least a portion of the side wall spacers (108). They have top surfaces that define a second plane above the first plane and comprise a doped crystalline semiconductor. The gate electrode has first side wall spacers disposed along opposing vertical walls.

INDEPENDENT CLAIMS are also included for the following:

(a) a method for making a junction, comprising: forming a patterned structure on a surface of a substrate, the substrate being of a first conductivity type; isotropically etching the substrate such that a ***recess*** in the substrate is formed, the ***recess*** including a portion that underlies the patterned structure and a surface; and selectively forming a layer of a first material having a second conductivity type in the ***recess*** ; and

(b) a method of making a transistor, comprising forming a dielectric on a first surface of a wafer; forming a conductive layer overlying the dielectric; patterning the conductive layer and dielectric to form a gate structure; forming ***recesses*** adjacent and partially subjacent the gate structure; and in a continuous operation, back filling the ***recesses*** with doped crystalline material, the back filling comprising forming crystalline material of at least a first conductivity.

USE - Microelectronic structures e.g., ***field effect*** transistors.

ADVANTAGE - The structure provides a short ***channel*** length and low source/drain ***extension*** resistivity. It is operable to produce high drive currents without suffering from the short ***channel*** effects that produce significant levels of off-state current.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic cross-section illustrating the structure of a wafer after an alternative process flow in which the back-filling of the ***recesses*** includes forming layers of two conductivity types. Substrate 102

Dielectric 104

Gate electrode 106

Side wall spacers 108

Source and drain terminals 110 Dwg.6/7

WO 200030169 A1UPTX: 20000811

EXAMPLE - In an EMBODIMENT of the structure, a body disposed within the substrate has two portions, second side wall spacers being adjacent to the first side wall spacers, and a metal salicide in an upper portion of the gate electrode and an upper portion of the source/drain terminals. The first portion is of a first conductivity and a first doping profile, and includes counterdopants. The second portion is of the second conductivity type and a second doping profile, and is free of counterdopants. A transition between the first and second doping profiles is abrupt. The patterned structure comprises a dielectric layer, where a conductive material is disposed over the layer.

Technology

WO 200030169 A1UPTX: 20000811 TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Material: The gate electrode comprises ***polysilicon*** disposed over the gate electrode, and crystalline silicon of a first conductivity type disposed over the ***polysilicon***. It further comprises a crystalline silicon of a second

conductivity type. The source/drain terminals comprise p-type silicon, n-type silicon, p-type silicon germanium, or n-type silicon germanium. The substrate comprises silicon doped to have the first conductivity type. The first and second materials comprise doped silicon germanium, where the second material has a ***thickness*** less than that of the first. Preferred Method: The etching passivates the surface of the ***recess*** and comprises exposing the substrates to sulfur hexafluoride (SF6) and helium (He) in a radio frequency (RF) etching system. Forming a ***recess*** comprises placing the substrate in a parallel plate reaction chamber with a gap of approximately 1.1 cm, an RF power of approximately 50-200 W, a pressure greater than approximately 500 mTorr, and a plasma etching with SF6 and He. The method further comprises depositing the first layer of doped crystalline material until a vertical ***distance*** between the top surface and surface of the substrate is greater than that between the top surface of the gate insulator and surface of the substrate.

Manual Codes

CPI: L04-C02; L04-C11; L04-C11C; L04-C12; L04-E01A EPI: U11-C05F1; U11-C18A3; U12-D02A

☐ **L37 ANSWER 15 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

2000-085643 [07] WPIX Full Text

Title

Formation of shallow trench isolation with raised field oxide regions.

Author/Inventor

CHAN, L; QIAN, G; QINGHUA, Z; SUAN, T P; GANG, Q; TAN, P S; ZHONG, Q

Patent Assignee/Corporate Source

(CHAR-N) CHARTERED SEMICONDUCTOR MFG LTD PTE

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 6001706	A	19991214	(200007)*		10	H01L021-76
SG 73543	A1	20000620	(200039)			H01L021-76

International Patent Classification ICM H01L021-76

Abstract

US 6001706 A UPAB: 20000209

NOVELTY - Shallow ***trench*** isolation is formed with raised field oxide regions which are self-aligned and ***extend*** over the edges of device areas to eliminate the wrap-around corner effect.

DETAILED DESCRIPTION - The method comprises:

- forming thermal pad oxide;
- adding ***polysilicon*** and a nitride hard mask;
- pattern etching the layers to form ***trenches*** in the substrate;
- forming thermal oxide liner in the ***trenches*** while forming ***thicker*** oxide on the ***polysilicon*** sidewalls ***extending*** over the edges of device areas;
- adding a conformal CVD oxide fill layer;
- chemical-mechanical polishing back to the hard mask;
- removing the hard mask by selective etching;
- and removing the ***polysilicon*** over the device areas.

USE - In fabrication of integrated circuits.

ADVANTAGE - Shallow ***trench*** isolation is formed without the wrap around corner effects that result from ***recesses*** in the field oxide after chemical-mechanical polishing, and produce sub-threshold hump'.

DESCRIPTION OF DRAWING(S) - The drawings show stages in the process of the invention.

Pad oxide 12

Polysilicon 13
Nitride hard mask 14
Liner oxide 16
Oxidised ***polysilicon*** 16'
Gap fill oxide 18
FET gate ***oxide*** 20
Gate electrode 22
7,8A,9A,10A,11,12/13

Manual Codes
CPI: L04-C12C EPI: U11-C08A3

☐ **L37 ANSWER 16 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number
1999-418376 [35] WPIX Full Text

Title
Trench -free buried contacts to semiconductor devices, particularly for SRAMs.

Author/Inventor
LEE, J; LIAW, J

Patent Assignee/Corporate Source
(TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5926706	A	19990720	(199935)*		12	H01L021-8244

International Patent Classification ICM H01L021-8244

Abstract
US 5926706 A UPAB: 19990902
NOVELTY - Buried contacts with diffused contact regions are formed on semiconductor integrated circuits. The method uses the ***etch back*** of an opening in the photoresist contact mask and a subsequent angular implant to ***extend*** the diffused contact regions to reduce the sheet resistance between the buried contacts and the ***FETs***.

DETAILED DESCRIPTION - The method comprises forming a gate oxide (14) on the device areas formed on a silicon substrate, the device areas being surrounded and electrically isolated from each other by field oxide regions. A first ***polysilicon*** layer (16) is deposited on the device areas and field oxide regions, and openings formed in the ***polysilicon*** and gate oxide over the device areas using a patterned first photoresist mask. The photoresist mask is isotropically etched in the openings thereby ***recessing*** the mask and exposing peripheral portions of the ***polysilicon*** layer along the edge of the openings. A first N+ ion implantation is implanted at an angle of 15-45 deg. to the substrate through the openings and the peripheral portions to ***extend*** under the edge of the mask, thereby forming diffused contact regions (22) ***extending*** under the gate oxide. A second P ion implantation is performed in the openings ***extending*** below the first N+ ion implantation, and a second ***polysilicon*** layer and a ***silicide*** layer consecutively deposited to form a polycide layer (24'') over the device openings and on the field oxide regions. A patterned second photoresist mask is used to pattern the polycide layer and the first ***polysilicon*** layer to form gate electrodes (24') for the ***FETs*** , and patterned electrical connections to the diffused contact regions.

USE - Making ***trench*** free buried contacts to diffused contact regions for ***field effect*** transistors (***FETs***) on a semiconductor substrate. Particularly applicable to SRAMs for reducing the design rules for achieving high density memories with better circuit performance.

ADVANTAGE - A very manufacturable and cost effective process for making

reliable buried contacts having a low sheet resistance between them and the source or drain areas of ***FETs***.

DESCRIPTION OF DRAWING(S) - The drawing shows a buried contact to a ***FET*** made according to the invention. Gate oxide 14

Polysilicon layer 16

Diffused contact region 22

Gate electrode 24'

Polycide lines 24''

Source/drain areas 28

Sidewall spacers 32

Dwg.14/14

US 5926706 A UPTX: 19990902

EXAMPLE - Lightly N+ doped source/drain areas (28) are implanted adjacent to the gate electrode (24') and into the extended diffused region (22) to provide a low sheet resistance between the buried contact and the FET. A sidewall insulating layer is deposited and anisotropically etched back to form sidewall spacers (32) on the sidewalls of the gate electrode (24'), and also on the sidewall of the polycide interconnecting line (24''). Heavily N+ doped FET source/drain contact areas (28) are formed to complete the buried contact region (22) contiguous with the source/drain areas (28) resulting in low sheet resistance.

Technology

US 5926706 A UPTX: 19990902 TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred material: The first ***polysilicon*** layer is in-situ doped N+ and is deposited 300-1000 ***Angstrom thick***. The first photoresist mask is ***recessed*** a ***distance*** of 500-2000 ***Angstrom***. The second ***polysilicon*** layer is N+ doped to a concentration of 1.0E20-1.0E21 atoms/cm3, and is deposited 500-1500 ***Angstrom thick***. The isotropic etching of the patterned first photoresist layer and the first ion implantation provide a greater latitude in aligning the second ***polysilicon*** layer over the openings for the buried contacts, and further reduces the sheet resistance between the buried contacts and the ***FETs***. The first N+ ion implantation is P31. The second P ion implantation is B11. The ***silicide*** layer is tungsten ***silicide*** , 750-1500 ***Angstrom thick***.

Manual Codes

CPI: G06-D06; L03-G04A; L04-C02B; L04-C06A; L04-C10B; L04-C11; L04-C12A; L04-E01A EPI: U11-C18B5

☐ **L37 ANSWER 17 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1999-290418 [25] WPIX Full Text

Title

Manufacture of a recessed gate field effect semiconductor device.

Author/Inventor

HUTCHINGS, K M; WHIGHT, K R

Patent Assignee/Corporate Source

(PHIG) KONINK PHILIPS ELECTRONICS NV; (PHIG) PHILIPS ELECTRONICS UK LTD

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
(1) EP 918353	A1	19990526	(199925)*	EN	13	H01L021-336

International Patent Classification ICM H01L021-336

ICS H01L021-331; H01L029-739; H01L029-78

Abstract

EP 918353 A UPAB: 19990719

NOVELTY - A ***recessed*** gate ***field effect*** device is manufactured by forming doped regions at the side of the gate in a self-aligned manner using sidewalls

of doped material as a diffusion dopant source.

DETAILED DESCRIPTION - A ***recessed insulated*** gate ***field effect*** device is formed in a substrate having a first region of first type separated from the surface by a second region of second type. The device is formed by etching a ***groove*** into the first region, adding a ***thin*** gate insulator and an oxidisable conductor to form an insulated gate bounded by a ***channel*** in the second region, the gate structure being made to ***extend*** above the surface to define a step by oxidizing the gate conductive material to form an insulating cap. Third regions of first type are then formed in a self-aligned manner adjacent the step by providing doped layer sidewalls at the step and causing dopant to diffuse into the underlying second region.

USE - Especially as a ***trench*** power ***MOSFET***.

ADVANTAGE - The third regions (source/drain regions) are formed in a self-aligned manner, allowing an increase in cell packing density where the device is a power device consisting of many parallel-connected cells without having to rely on the use of birds beak regions as a mask to define the third regions.

DESCRIPTION OF DRAWING(S) - The drawings show the ***MOSFET*** device at intermediate and final stages of the method of the invention

First region of first type 2
Second region of second type 3
Insulated gate structure 8
Step 15
Insulating cap region 9
Third region of first type 11
Sidewalls formed of a doped layer, preferably doped ***polysilicon*** 10

Dwg.5,8/11

Manual Codes

CPI: L04-C07E; L04-C12A; L04-E01B1; L04-E02 EPI: U11-C18A3; U12-D02A9; U12-Q

☐ **L37 ANSWER 18 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1997-131809 [12] WPIX Full Text

Title

Mfg. a buried structure SRAM cell - increases integration density, controls channel width and avoids birds beak encroachment.

Author/Inventor

KO, J; WEN, J

Patent Assignee/Corporate Source

(UNMI-N) UNITED MICROELECTRONICS CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5602049	A	19970211	(199712)*		9	H01L021-70

International Patent Classification ICM H01L021-70

ICS H01L027-00

Abstract

US 5602049 A UPAB: 19981203

Mfg. a buried structure SRAM cell comprises forming a doped well in a Si substrate, forming, masking and etching a pad oxide to form source/drain ***trenches*** and doping the substrate to raise punchthrough voltage between these ***trenches***. A silica layer is formed on a ***trench*** surface and the ***trenches*** filled and substrate covered by depositing a ***poly -Si*** layer (21). This is ***etched back*** to form ***recesses*** at the ***trenches*** , the silica partly removed by wet etching and the whole covered by an oppositely doped ***poly -Si*** layer to form a PN junction by diffusion. The first poly layer is ***etched back*** to form

MOSFET source/drain regions and gate ***trenches*** (311) formed and filled with dielectric to control ***channel width***. ***Trenches*** are masked and dopants implanted to form a ***channel*** stop region at a gate ***trench*** wall of the pass transistor, gate ***trenches*** are ion-implanted to adjust a ***MOSFET*** threshold voltage and gate oxide grown overall and etched to form a buried contact region. A second doped ***poly -Si*** layer is deposited and ***etched back*** to form a ***MOSFET*** gate electrode using gate oxide as end-pt. detector and an interpoly dielectric layer formed and masked and etched to form vias for poly-loads which are formed by depositing a third ***poly -Si*** layer and patterning.

USE - In the mfr. of high density buried structure SRAM cells

ADVANTAGE - There is a high cell ratio without extra area, the ***MOSFET channel width*** is controlled and a more planar topography is obtd.

Dwg.3H/6

Manual Codes

CPI: L03-G04A; L04-C02B; L04-C07; L04-E01B1 EPI: U11-C18B5; U13-C04B1B

☐ **L37 ANSWER 19 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1994-048095 [06] WPIX Full Text

Title

Recessed gate field effect power MOS device mfg. method e.g. power MOSFET , IGBT, MOS controlled thyristor - using sidewall spacer on trenching protective layer in self-aligned process to control pinched p-type base width lateral extent, with trenching protective layer formed by oxide on polysilicon on thin thermal oxide.

Author/Inventor

MEYER, T O; MOSIER, J W; PIKE, D A; TSANG, D W; TSANG, D

Patent Assignee/Corporate Source

(ADPO-N) ADVANCED POWER TECHNOLOGY INC

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5283201	A	19940201	(199406)*		21	H01L021-00
WO 9403922	A1	19940217	(199408)	EN	42	H01L021-265
EP 654173	A4	19960814	(199702)			H01L021-00
DE 69333100	E	20030821	(200362)			H01L021-265

International Patent Classification ICM H01L021-00; H01L021-265

ICS H01L021-02

Abstract

US 5283201 A UPAB: 20030928

The ***recessed*** gate power ***MOSFET*** process involves using a substrate (20) including a P-body layer (26), N-drain layer (24), with e.g. an optional P+ layer (22) for an IGBT. A trenching protective layer formed on the substrate upper surface is patterned to define exposed areas as stripes or a matrix, and protected areas. Sidewall spacers (44) of predetermined ***thickness*** with inner surfaces (48) contact the protective layer sidewalls. A ***trench*** is formed in substrate areas with sidewalls aligned to the sidewall spacer outer surfaces and ***extending*** into the P-body layer to a preset depth. Gate oxide (60) is formed on the ***trench*** walls and gate ***polysilicon*** (62) refills the ***trench*** to a level near the substrate upper surface.

Oxide between sidewall spacers covers ***polysilicon*** Removing the protective layer exposes upper substrate surface between spacer inner surfaces. This area is doped to form a source layer over the body layer and then ***trenched*** to form a second ***trench*** having sidewalls aligned to the spacer inner surfaces. The second ***trench*** defines vertically-oriented source and body layers (86, 90) stacked

along gate oxide layer to form vertical ***channels*** on opposite sides of the second ***trench***.

USE/ADVANTAGE - Vertical ***channel*** power MOS structure; rectangular or U-shaped ***groove***. Maintains both series source resistance and vertical ***channel*** resistance; avoids LOCOS stress. Dwg.13/24

Manual Codes

EPI: U11-C18A2; U11-C18A3; U11-C18B2; U12-D01A1; U12-D01B1; U12-D02A9

☐ **L37 ANSWER 20 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1993-287788 [36] WPIX Full Text

Title

Lightly doped drain field effect transistor with inverted T-gate electrode - has consecutive, conformal layers of poly silicon , metal and nitride or oxide deposited to fill recess in composite interconnect layer on top of trench - isolated region of.

Author/Inventor

HSU, L L; OGURA, S; SHEPARD, J F; TSANG, P J

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5241203	A	19930831	(199336)*		7	H01L029-76

International Patent Classification ICM H01L029-76

ICS H01L023-48; H01L029-94; H01L031-062

Abstract

US 5241203 A UPAB: 19931122

The lightly doped drain, ***field effect*** transistor with an inverted ''T''-gate structure includes a gate electrode disposed on a ***polysilicon*** pad in a stack opening. The inner edge of a lightly-doped source and drain region is aligned with the gate electrode, and its outer edge is aligned with an edge of the ***polysilicon*** pad.

The inner edge of a heavily-doped source and drain region is aligned with the edge of the edge of the ***polysilicon*** pad and its outer edge is aligned with the wall surface that forms the opening. The inner edge of a source and drain contact region is aligned with the wall and ***extends*** under the stack.

ADVANTAGE - Uses low resolution lithographic tools, sub- ***micron*** ***channel*** lengths and fully self-aligned features including source and drain. Has lightly doped regions overlain by inverted T-gate ***polysilicon*** layer, providing lower source drain series resistance than conventional LDD ***FET*** devices. Dwg.10/

Manual Codes

EPI: U11-C18A3; U12-D02A3

☐ **L37 ANSWER 21 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1992-216323 [26] WPIX Full Text

Title

Inverse T-gate FET transistor mfg. method - by selectively etching in two steps conformal layers of poly silicon metal and nitride or oxide deposited in recess on trench isolated region of substrate.

Author/Inventor

HSU, L L; OGURA, S; TSANG, P J; SHEPARD, J F

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 5120668	A	19920609	(199226)*		7	H01L021-265
EP 522991	A1	19930113	(199302)	EN	8	H01L021-336

International Patent Classification ICM H01L021-265; H01L021-336

Abstract

US 5120668 A UPAB: 19931122

The method of forming a ***field effect*** transistor having an inverted ''T''-shaped gate structure on an isolated device region, involves forming a multi-layer stack of ***polysilicon*** , metal, and a dielectric over the device region, and etching an aperture in the stack to expose a surface portion of the device region. A gate oxide layer is formed on the exposed portion of the device region, and consecutive conformal layers of ***polysilicon*** , a metal and a dielectric are formed, filling the aperture.

The conformal layers are polished back to the surface of the dielectric in the stack. The conformal layers are etched within the aperture with a first reactive ion etching (RIE) process that preferentially etches ***polysilicon*** and terminates this first etch when the remaining ***polysilicon*** in the aperture is at a depth where it will be removed to the oxide layer by the next etching step. The conformal layers are then within the aperture with a second reactive ion etch process that preferentially etches metal to form a T-gate structure. Ions are implanted through the aperture to form a ***field effect*** transistor inlcuding source and drain regions each having a lightly doped region ***extending*** underneath of the T-gate structure.

USE/ADVANTAGE - For mfr. of self-aligned tightly doped drain transistor, partic. inverse T-gate structure with sub-***micron channel*** lengths. Uses relatively low resolution lithographic process.

3,5,10/11

3,5,10/11

Manual Codes

EPI: U11-C18A3; U12-D02A3

☐ **L37 ANSWER 22 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1990-290010 [38] WPIX Full Text

Title

Self-aligned cross point LDD trench transistor - has improved short channel effects and is useful in ROM and DRAM cells.

Author/Inventor

DHONG, S H; HWANG, W; LU, N C; LU, N C C

Patent Assignee/Corporate Source

(IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
US 4954854	A	19900904	(199038)*			
CA 2006745	A ..	19901122	(199107)			
JP 03004560	A	19910110	(199108)			
CA 2006745	C	19930615	(199329)			H01L029-76
EP 399191	B1	19940824	(199433)	EN	16	H01L029-784
DE 69011736	E	19940929	(199438)			H01L029-784

International Patent Classification H01L021-82; H01L027-10; H01L029-78

ICM H01L029-76; H01L029-784

ICS H01L021-82; H01L027-10; H01L027-108; H01L029-78

Abstract

US 4954854 A UPAB: 19941013
A self-aligned, slightly doped drain/source ***field effect trench*** transistor device comprises a semiconductor substrate having a lower n+ portion (10), an upper epitaxial lightly doped n- portion (12), a p well (15) in the upper portion, and at least one ***poly -Si*** -filled ***trench extending*** from the well surface into the well, with a layer of gate oxide on the ***trench*** bottom and sidewalls isolating it from the well. There is a source junction (26) in the wall below the ***trench*** , a diffusion region forming a first drain junction region (18), being heavily n++ doped, on the surface of the well around the ***trench*** , and a second n+ LDD region (24) in the well near the first drain and self-aligned with the upper sidewalls of the ***trench***. Also a ***poly -Si*** word line element is disposed over the filled ***trench***.

USE/ADVANTAGE - A self-aligned LDD ***trench*** transistor (claimed) is provided which has improved short ***channel*** effect and punch-through characteristics, lower overlap capacitance and mobility degradation, and minimised source and drain incremental resistance. The transistor is useful in ROM and DRAM cells. @(13pp Dwg.No.1/15)@ 1/15

Abstract, Equivalent

EP 399191 B UPAB: 19941010 A process for fabricating self-aligned drain/source ***field effect trench*** transistor device comprising the steps of: Step 1) on semiconductor substrate of a first conductivity type material (10) having a layer of epitaxial material (12) thereon, implanting dopants to form a retrograde well region (15) of a second conductivity type in said epitaxial material, Step 2) forming oxide isolation regions (16) in the surface of said well region (15) and implanting dopants between said isolation regions (16) to form a diffusion region (18) of a first conductivity type to provide first drain junction regions, Step 3) etching a vertical ***trench*** (20) through said diffusion region (18) into said well region (15), Step 4) implanting dopants into the vertical sides of said ***trench*** (20) using a low angle oblique ion implantation technique, Step 5) forming layers of silicon nitride masking material on the vertical sidewalls of said ***trench*** (20) ***extending*** below a point located below the level of said diffusion region (18) formed in Step 2, Step 6) forming self-aligned second drain junction regions (24) having a doping concentration smaller than that of said diffusion region (18) on the side-walls of said vertical ***trench*** (20) above said silicon nitride mask layers (22) and form buried source junction (26) below the bottom of said ***trench*** (20) by using said low angle oblique ion implantation technique, Step 7) growing oxide (16A) on said ***recessed*** oxide regions and on the bottom of said ***trench*** (20) over said source junction (26), Step 8) removing said silicon nitride mask layer (22) from said vertical ***trench*** sidewalls and growing a ***thin*** gate oxide (30) on said vertical ***trench*** sidewalls, and Step 9) filling said ***trench*** (20) with ***polysilicon*** and depositing ***polysilicon*** over said filled ***trench*** and over said ***recessed*** oxide regions and well surface to form transfer gate (32) and wordline elements (33). Dwg.1/15

Manual Codes

CPI: L03-G04A; L04-E01A EPI: U11-C02J6; U12-D02A; U13-C04A; U13-C04B

☐ **L37 ANSWER 24 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1989-341718 [47] WPIX Full Text

Title

Topographic pattern delineated power MOSFET - has profile tailored recessed source, and dopant opaque layer of polysilicon deposited on gate oxide on silicon substrate to define pattern.

Author/Inventor

HOLLINGER, T G; MEYER, T O; MOSIER, J W; PIKE, D A; TSANG, D W

Patent Assignee/Corporate Source

(ADPO-N) ADVANCED POWER TECHNOLOGY INC

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
EP 342952	A	19891123	(198947)*	EN	24	
US 4895810	A	19900123	(199011)		21	
JP 02056937	A	19900226	(199014)			
US 5019522	A	19910528	(199124)			
US 5045903	A	19910903	(199138)			
US 5089434	A	19920218	(199210)			
CA 1305261	C	19920714	(199234)			H01L021-335
US 5182234	A	19930126	(199307)		18	H01L021-00
US 5256583	A	19931026	(199344)		18	H01L021-70
CA 1326567	C	19940125	(199409)			H01L021-336
CA 1326568	C	19940125	(199409)			H01L021-24
DE 68927309	E	19961114	(199651)			H01L029-08

International Patent Classification H01L021-28; H01L029-08

ICM H01L021-00; H01L021-24; H01L021-335; H01L021-336; H01L021-70; H01L029-08

ICS H01L021-02; H01L021-225; H01L021-28; H01L021-306; H01L021-308; H01L021-31; H01L021-467; H01L029-41; H01L029-78; H01L029-784

Abstract

EP 342952 A UPAB: 20020919

In the ***MOSFET*** , a dopant-opaque layer of ***polysilicon*** is deposited on gate oxide (26) on a silicon substrate (18, 20) to serve as a pattern definer. It controls successive P and N doping steps used to form operative DMOSFET regions within the substrate, a ***trench*** in the' silicon surface, and conductive structures (28, 30) atop the substrate. A source conductive layer (28) is deposited in the ***trench*** to electrically contact the source region (24) as a gate conductive layer (30) is deposited atop the gate oxide (26).

The tench sidewall is profile tailored using a novel O2-SF6 plasma etch technique. A planarising layer is used as a mask for selectively removing any conductive material deposited atop the oxide spacer.

ADVANTAGE - Eliminates incidence of fatal defects in power device. Dwg.2/21

Abstract, Equivalent

US 4895810 A UPAB: 19930923 The ***MOSFET*** includes a dopant-opaque layer of ***polysilicon*** deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabrication of the device. A ***trench*** is formed in the upper silicon surface and a source conductive layer is deposited to electrically contact the source region as a gate conductive layer is deposited atop the gate oxide layer. The ***trench*** sidewall is profiled tailored using a O2-SF6 plasma etch technique. An oxide sidewall spacer is formed on the sides of the pattern definer and gate oxide structure, before depositing the conductive material. A planarising layer is applied and used as a mask for selectively removing any conductive material deposited atop the oxide spacer. The ***polysilicon*** layer on the oxide is reduced in ***thickness*** during trenching. The sidewall spacers may be sized. ADVANTAGE - Reduced number of fatal defects in final semiconductor device.

US 5019522 A UPAB: 19930923 A dopant-opaque layer of ***polysilicon*** is deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabrication of the device. It provides control over successive P and N doping steps used to create the necessary operative junctions within a silicon substrate and the conductive structures formed atop the substrate. A ***trench*** is formed in the upper silicon surface and a source conductive layer is deposited to electrically contact the source region as a gate conductive layer is deposited atop the gate oxide layer. The ***trench*** sidewall is profile tailored

using a novel O2-SF6 plasma etch technique. An oxide sidewall spacer is formed on the sides of the pattern definer and gate oxide structure, before depositing the conductive material. A planarising layer is applied and used as a mask for selectively removing any conductive material deposited atop the oxide spacer. The ***polysilicon*** layer on the oxide is reduced in ***thickness*** during trenching so that any conductive material deposited atop the spacers protrude upward for easy removal of excess, conductive material. The sidewall spacers can be sized, either alone or in combination with profile tailoring of the ***trench*** , to control source-region ***width*** (i.e., parasitic pinched base ***width***) and proximity of the source conductor to the ***FET channel.*** USE/ADVANTAGE - For power ***MOSFET*** mfr.. Electrical contact between source conductive layer and source regions is enhanced by forming low-resistivity layer between them.

US 5045903 A UPAB: 19930923 The dopant-opaque layer of ***polysilicon*** is deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabrication of the device. A ***trench*** is formed in the upper silicon surface and a source conductive layer is deposited to electrically contact the source region as a gate conductive layer is deposited atop the gate oxide layer. The ***trench*** sidewall is profile tailored using a O2-SF6 plasma etch technique. An oxide sidewall spacer is formed on the sides of the pattern defined and gate oxide structures, before depositing the conductive material. A planarising layer is applied and used as a mask for selectively removing any conductive material depositioned atop the oxide spacer. The ***polysilicon*** layer on the oxide is reduced in ***thickness*** during trenching so that any conductive material deposited atop the spacers protrude upward for easy removal of excess, conductive material. The sidewall spacers can be sized, either alone or in combination with profile tailoring of the ***trench*** , to control source-region ***width*** (ie., parasitic pinched base ***width***) and proximity of the source conductor to the ***FET channel.*** ADVANTAGE - Electrical contact enhanced.

US 5089434 A UPAB: 19930923 A dopant-opaque layer of ***polysilicon*** is deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabrication of the device. It provides control over successive P and N doping steps used to create the necessary operative junctions within a silicon substrate and the conductive structure formed atop of the substrate. A ***trench*** is formed in the upper silicon surface and a source conductive layer is deposited to electrically contact the source region as a gate conductive layer is deposited atop the gate oxide layer. The ***trench*** sidewall is profile tailored using a novel O2-SF6 plasma etch technique. An oxide sidewall spacer is formed on the sides of the pattern definer and gate oxide structures, before depositing the conductive material. A planarising layer is applied and used as a mask for selectively removing any conductive material deposited atop the oxide spacer. The ***polysilicon*** layer on the oxide is reduced in ***thickness*** during trenching so that any conductive material deposited atop the spacers protrude upward for easy removal of excess, conductive material. The sidewall spacers can be sized, either alone or in combination with profile tailoring of the ***trench*** , to control source-region ***width*** (i.e., parasitic pinched base ***width***) and proximity of the source conductor to the ***FET channel.*** Electrical contact between the source conductive layer and the source regions is enhanced by forming a low-resistivity layer between them. USE - For mfg. power semiconductor device, esp. power ***MOSFET*** .

US 5182234 A UPAB: 19930923 A dopant opaque layer of ***polysilicon*** is deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabricatoin of the device. It provides control over successive P and N doping steps used to create the necessary operative junctions within a silicon substrate and the conductive structures formed on the substrate. A ***trench*** is formed in the upper silicon surface and a source conductive layer is deposited to electrically contact the source region as a gate conductive layer is deposited on the gate oxide layer. The ***trench*** sidewall is profile tailored

using a O2-SF6 plasma etch technique. An oxide sidewall spacer is formed on the sides of the pattern definer and gate oxide structures, before depositing the conductive material. A planarising layer is applied and used as a mask for selectively removiny any conductive material deposited on the oxide spacer. The ***polysilicon*** layer on the oxide is reduced in ***thickness*** during trenching so that any conductive material deposited on the spacers protrude upward for easy removal of excess, conductive material. The sidewall spacers can be sized, either alone or in combination with profile tailoring of the ***trench*** , to control source-region ***width*** (i.e. parasitic pinched base ***width***) and proximity of the source conductor to the ***FET channel***. Electrical contact between the source conductive layer and the source regions is enhanced by forming a low resistivity layer between them. ADVANTAGE - Increased yield. (Dwg.13c/7 13c/7
US 5256583 A UPAB: 19931213 A dopant-opaque layer of ***polysilicon*** is deposited on gate oxide on the upper substrate surface to serve as a pattern definer during fabrication of the device. It provides control over successive P and N doping steps used to create the necessary operative junctions within a silicon substrate and the conductive structures formed atop the substrate. A ***trench*** is formed in the upper silicon surface and a source conductive layer is depsited to electrically contact the source region as a gate conductive layer is deposited atop the gate oxide layer. The ***trench*** sidewall is profile tailored using a O2-SF6 plasma etch techniquie. An oxide sidewall sapcer is formed on the sides of the pattern definer and gate oxide structures, before depositing the conductive material. A planarizing layer is applied andused as a mask for selectively removing any conductive material deposited atop the oxide spacer. The ***polysilicon*** layer on the oxide is reduced in ***thickness*** during trenching so that any conductive material deposited atop the spacers protrude upward for easy removal of excess, conductive material. The sidewall spacers can be sized, either alone or in combination with profile tailoring of the ***trench*** , to control source-region ***width*** (ie., parasitic pinched base ***width***) and proximity of the source conductor to the ***FET channel***. Electrical cotact between the source conductive layer and the source regions is enhanced by forming a low-resistivity layer between them. ADVANTAGE - Increased yield of high current device. Dwg.2/21
EP 342952 B UPAB: 19961111 A method of employing a mask-surrogate pattern definer, of producing a vertical double-diffused ***MOSFET*** device (10) on the upper surface of a semiconductor substrate (11) including a gate oxide layer (26), said method including the following steps performed in the given order; providing a silicon substrate (11) having an upper surface, forming an oxide layer (26) on the upper surface of the substrate having a first predetermined ***thickness*** , forming a dopant protective layer (32) over the oxide layer in a second predetermined ***thickness*** , forming a defined outline characteristic in such protective layer by selectively removing a portion of the dopant protective layer, exposing an upper surface portion of the substrate (11) and opposite sides of the protective layer (32) and underlying oxide layer (26) along a boundary determined by the defined outline characteristic, doping the substrate successively with dopant ions of opposite polarity type (42,50) to form a first diffusion and a second diffusion providing a double-diffused, vertical ***field effect*** transistor positioned under the oxide layer and arranged to define a source region (24) subjacent the defined outline characteristic, a drain region (25) spaced laterally from the source region (24) beneath the end oxide layer (26) and ***extending*** downward into the bulk of the substrate, and a conduction ***channel*** (22) positioned between th source and drain regions and operable upon inversion to conduct current between the source and drain regions, forming an insulative sidewall spacer (62) on each side of the dopant protective layer (32) and the oxide layer underlying it (26) with a ***thickness*** defining a lateral offset from said defined outline characteristic and a vertical ***dimension*** approximately equal to the sum of said first and second predetermined

thicknesses , forming a ***trench*** (63) having a base and sidewalls in the exposed upper surface portion of the substrate (11), removing th protective layer (32) during the ***trench*** formation thus forming a ***recess*** between the sidewall spacers forming a gate conductive layer (30) on the oxide layer (26) and a source conductive layer (28) on at least the base of the ***trench*** (63) such that the source conductive layer (28) contacts the source diffusion region (24), in which method, the doping step includes introducing dopant ions for the source region prior to the ***trench*** -forming step and diffusing the dopant ions after the ***trench*** -forming step. Dwg.1/21

Manual Codes

EPI: U11-C02A2; U11-C02J6; U12-D02A

☐ **L37 ANSWER 25 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1987-275645 [39] WPIX Full Text

Title

Production of semiconductors, especially FET - by applying insulating film containing silicon nitride to leave cut-out areas, and forming silicon film and active regions.

Patent Assignee/Corporate Source

(NITE) NIPPON TELEGRAPH & TELEPHONE CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
NL 8700279	A	19870901	(198739)*		19	
JP 62230056	A	19871008	(198746)			
NL 190388	B	19930901	(199338)		11	H01L021-20

International Patent Classification ICM H01L021-20

ICS H01L029-06; H01L029-78

Abstract

NL 8700279 A UPAB: 19931123

Production comprises coating the surface of a semiconductor substrate with an insulating layer comprising a film of silicon nitride or a film containing silicon nitride as a principal component, to form a surface layer with a predetermined, pattern of cut-out areas which are not covered by the insulating layer and through which the semiconductor substrate is exposed; forming a silicon film in the cut-out areas ***extending*** across the exposed semiconductor substrate to the neighbouring surrounding insulating layer; and forming active areas on the semiconductor device on the silicon film.

USE/ADVANTAGE - The process is esp useful for production of semi-conductor substrates for ***field effect*** transistors which can be miniaturised and which have a reduced parasitic capacity and improved reliability of contact between a diffused layer and a metal electrode.

Dwg.1A/6

Abstract, Equivalent

NL 190388 B UPAB: 19931123 Fabricating a semiconductor device of the ***MOSFET*** type comprises selective coating of an exposed surface of a semiconductor substrate with an insulating layer such that a ***recess*** region of the substrate is left exposed by the insulating layer, with the simultaneous formation of a epitaxial Si film on the exposed ***recess*** region and a ***polycrystalline Si*** film on the insulating layer, while a form is retained having an ***recess*** , at a temp. above 700 deg.C, and forming a whole ***channel*** region and part of diffused source- and drain regions in the epitaxial Si film and the remainder of diffused source- and drain layer regions in the ***polycrystalline Si*** film. The insulating layer consists of a Si nitride contg. film or upper surface and side surface of the insulating film are covered with a Si nitride contg. film, and the epitaxial

Si film and ***polycrystalline Si*** film are formed to a ***thickness*** of less than 0.3 micrometres. USE/ADVANTAGE - The process allows formation of a ***polycrystalline Si*** film with a smooth surface which permits the prodn. of devices with a microstructure. Dwg.0/6

Manual Codes

CPI: L04-C12B; L04-E01A EPI: U11-C18A; U12-D02A

☐ **L37 ANSWER 26 OF 28 WPIX COPYRIGHT 2004 THOMSON DERWENT on STN**

Accession Number

1984-019330 [04] WPIX Full Text

Title

IC containing completely dielectrically isolated regions - is formed by undercut etching and oxidising from trenches between recessed oxide strips.

Author/Inventor

LECHATON, J S; MALAVIYA, S D; SCHEPIS, D J; SRINIVASAN, G

Patent Assignee/Corporate Source

(IBMC) IBM CORP

Patent Information

PATENT NO.	KIND	DATE	WEEK	LA	PG	MAIN IPC
EP 98374	A	19840118	(198404)*	EN	28	
JP 59008346	A	19840117	(198408)			
US 4502913	A	19850305	(198512)			
US 4661832	A	19870428	(198719)			
JP 63047337	B	19880921	(198841)			
DE 3380837	G	19891214	(198951)			

International Patent Classification B44C001-22; C03C015-00; H01L021-76; H01L027-04

Abstract

EP 98374 A UPAB: 19930925

Isolated monocrystal Si IC regions are formed by (a) providing a monocrystal Si region (14) isolated at its surface from other regions by two parallel dielectric strips (18), and having a buried n+ region (12) ***extending*** across the body parallel to the surface at least below the dielectric strips; (b) anisotropically etching parallel pairs of ***trenches extending*** through the n+ region between the strips; so the n+ region is pref. etched to ***undercut*** overlying Si (14) and ***trenches*** are spaced so each etched n+ region approaches the other of the pair; (c) thermally oxidising exposed Si ***trench*** surfaces until the n+ region between ***trenches*** is completely oxidised; and (d) filling the ***trenches*** with dielectric material (36).

An IC having completely dielectrically isolated devices comprises (i) an Si substrate (10) having an n+ layer (12) and an epitaxial layer (14); (ii) ***recessed*** oxide isolation regions (18) laterally isolating portions of the epitaxial layer; (iii) insulator filled ***trenches*** (36) between ***recessed*** oxide regions, ***extending*** from the surface into the body; (iv) oxidised n+ Si regions (32) between ***trenches*** and ***recessed*** oxide isolation; and (v) connections between device elements in isolated regions forming the IC.

The complete dielectric isolation provide optimum isolation for IC elements, pref. bipolar or ***field effect*** devices, and is formed in a simplified manner.

2,3,4/10

Abstract, Equivalent

EP 98374 B UPAB: 19930925 Method for fabricating a fully dielectrically isolated region for an integrated circuit in a monocrystalline silicon body comprising: -providing a monocrystalline silicon region on one major surface of a monocrystalline silicon body dielectrically isolated at said surface from other such regions by two parallel recelled strips of dielectric material, said

silicon body having an N+ sub-region spaced from said major surface and ***extending*** parallel to said major surface at least substantially across said body and below said dielectric strips, anisotripically etching parallel pairs of ***trenches*** ***extending*** , within said monocrystalline region, between said dielectric stips and through said N+ subregion, the etch rate of said anisotropic etching being adjusted to cause a preferential etching of said N+ sub-region so that a portion of the said N+ region is removed and monocrystalline silicon remains above this removed portion. the spacing of said ***trenches*** being chosen such that said preferential etching of said N+ sub-region from each ***trench*** closely approaches the other of the pair, thermally oxidizing the exposed silicon surfaces of said ***trenches*** until the said N+ sub-region between said ***trenches*** is totally oxidized to silicon dioxide, and filling said ***trenches*** with dielectric material to produce said dielectrically isolated silicon region.

US 4502913 A UPAB: 19930925 Total dielectrically isolated integrated circuit is in a monocrystalline Si body which incorporates two parallel regions of dielectric material so that isolated regions of monocrystalline Si are formed. An N+ sub-region (12) spaced from the surface ***extends*** across the body below the dielectric strips. Parallel pairs of ***trenches*** (20) between the dielectric strips and through the sub-region are formed by anisotropic etching in which the sub-region is etched preferentially so that ***polycrystalline Si*** remains above the removed N+ region, and the spacing of the ***trenches*** is such that the preferential etching of the sub-region from each ***trench*** approaches the other of the pair. Exposed Si surfaces are oxidised until the sub-region between the ***trenches*** form Si dioxide, and the ***trenches*** are filled with dielectric material. Semiconductor devices are formed in the isolated Si region and similar devices in the other region are connected to them. USE/ADVANTAGE - Bipolar integrated circuit with a fully isolated dielectric structure.

US 4661832 A UPAB: 19930925 Integrated circuit with completely isolated semiconductor devices has an epitaxial Si layer of predetermined ***thickness*** on a Si layer of predetermined ***thickness*** on a Si substrate. ***Recessed*** oxide isolation regions in the epitaxial layer completely isolate regions of the epitaxial layer, and insulator filled ***trenches*** ***extend*** between the ***recessed*** oxide isolation regions and from the surface of the substrate. The ***trenches*** contact the ***recessed*** regions and are deeper than the epitaxial layer ***thickness*** and an oxide layer between the filled ***trenches*** and the ***recessed*** isolation regions, and deeper than the ***trench*** depth. Semiconductor devices in selected isolated epitaxial regions are connected electrically to form an integrated circuit. USE - Mfr. of NPN bipolar devices or ***MOSFET*** devices.

Manual Codes

CPI: L03-D03 EPI: U11-C05B; U11-C07; U11-C08

☐ **L37 ANSWER 27 OF 28 JAPIO (C) 2004 JPO on STN**

Accession Number

2002-158355 JAPIO Full Text

Title

SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

Author/Inventor

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Patent Assignee/Corporate Source

NEC KANSAI LTD

Patent Information

JP 2002158355 A **20020531** Heisei

Priority Application Information

JP 2000-353072	20001120

International Patent Classification
ICM H01L029-78
ICS H01L021-8234; H01L027-088; H01L021-336

Abstract
PROBLEM TO BE SOLVED: To solve the problem that a ***channel*** layer as a ***MOSFET*** is not normally formed due to a lower surface of a gate electrode than a diffusion depth of a source region caused by overetching of a ***polysilicon*** film in a U-shaped ***groove*** when a method for manufacturing a conventional low withstand ***MOSFET*** of embedding the gate electrode excepting the ***polysilicon*** film only in the ***groove*** by ***etching back*** by laminating the ***polysilicon*** film on the surface of the epitaxial layer formed with the ***groove*** when an intermediate pressure or more ***MOSFET*** needing widening of a ***width*** of the U-shaped ***groove*** is manufactured as compared with the low withstand ***MOSFET***. SOLUTION: A method for manufacturing the semiconductor device comprises the steps of embedding and forming the gate electrode 46 in the U-shaped ***groove*** 43, and embedding and forming a ***polysilicon*** layer 54 in a ***recess*** of the electrode 46 via a ***thin*** silicon oxide film 53.

☐ **L37 ANSWER 28 OF 28 JAPIO (C) 2004 JPO on STN**

Accession Number
1988-128758 JAPIO Full Text

Title
FIELD -EFFECT TRANSISTOR

Author/Inventor
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Patent Information
JP 63128758 A **19880601** Showa

Priority Application Information

JP 1986-276127	19861119

International Patent Classification ICM H01L029-80
H01L029-44; H01L029-48

Abstract
PURPOSE: To reduce the parasitic resistance, especially the source resistance, to shorten the length of a gate and to reduce a short- ***channel*** effect by providing an n-type layer formed from the surface of a semi-insulating GaAs semiconductor substrate down to a prescribed depth, and an n<SP>+</SP> source region and a drain region formed in contact with a gate electrode buried into a ***recess*** formed from the surface of the n-type layer to a position before its bottom, and in contact with an insulating layer surrounding the circumferential side of the gate electrode. CONSTITUTION: A mask 22, for injection use, of SiO<SB>2</SB> is formed on an semi- insulating GaAs substrate 10, and ions of Si are implanted. As a replacement for the mask 22 for implantation use, a mask 24 for etching use is formed; a ***recess*** 26 for formation of a gate part is formed ; ions for a ***channel*** (n-layer) use are implanted; the assembly is annealed. SiO<SB>2</SB> is deposited; the deposited layer is etched over the whole ***thickness***. A layer 28 where tungsten ***silicide*** is deposited is coated with a photoresist layer; a resist layer 30 and the ***WSi*** <SB>x</SB> layer 28 are ***etched back*** over their ***thickness*** on n<SP>+</SP> layers 12a, 12b. An SiO<SB>2</SB> layer 32 is formed on the surface; windows for a source and a drain are opened; AuGe/Au is deposited; a source electrode and a drain electrode S, D are formed.